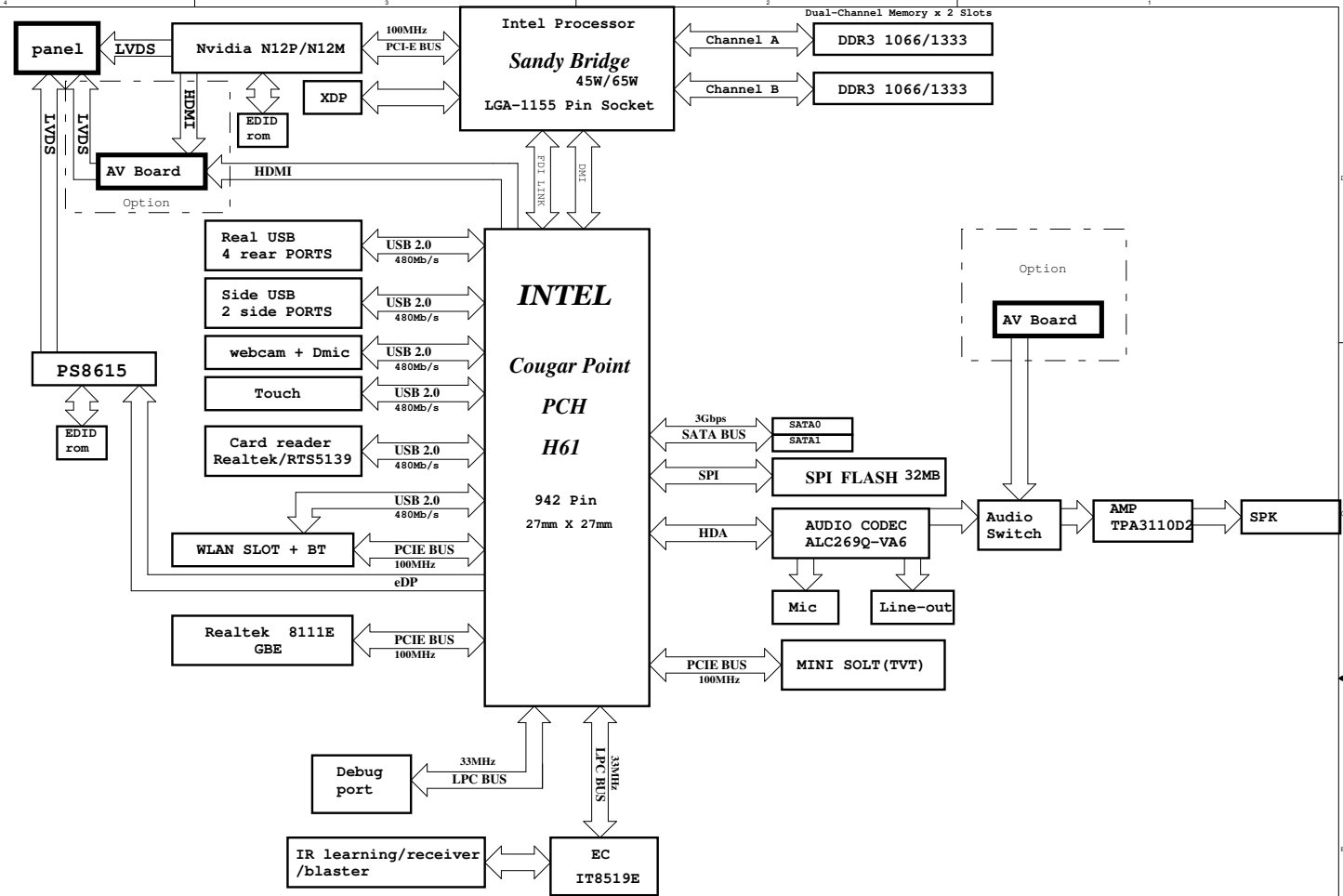
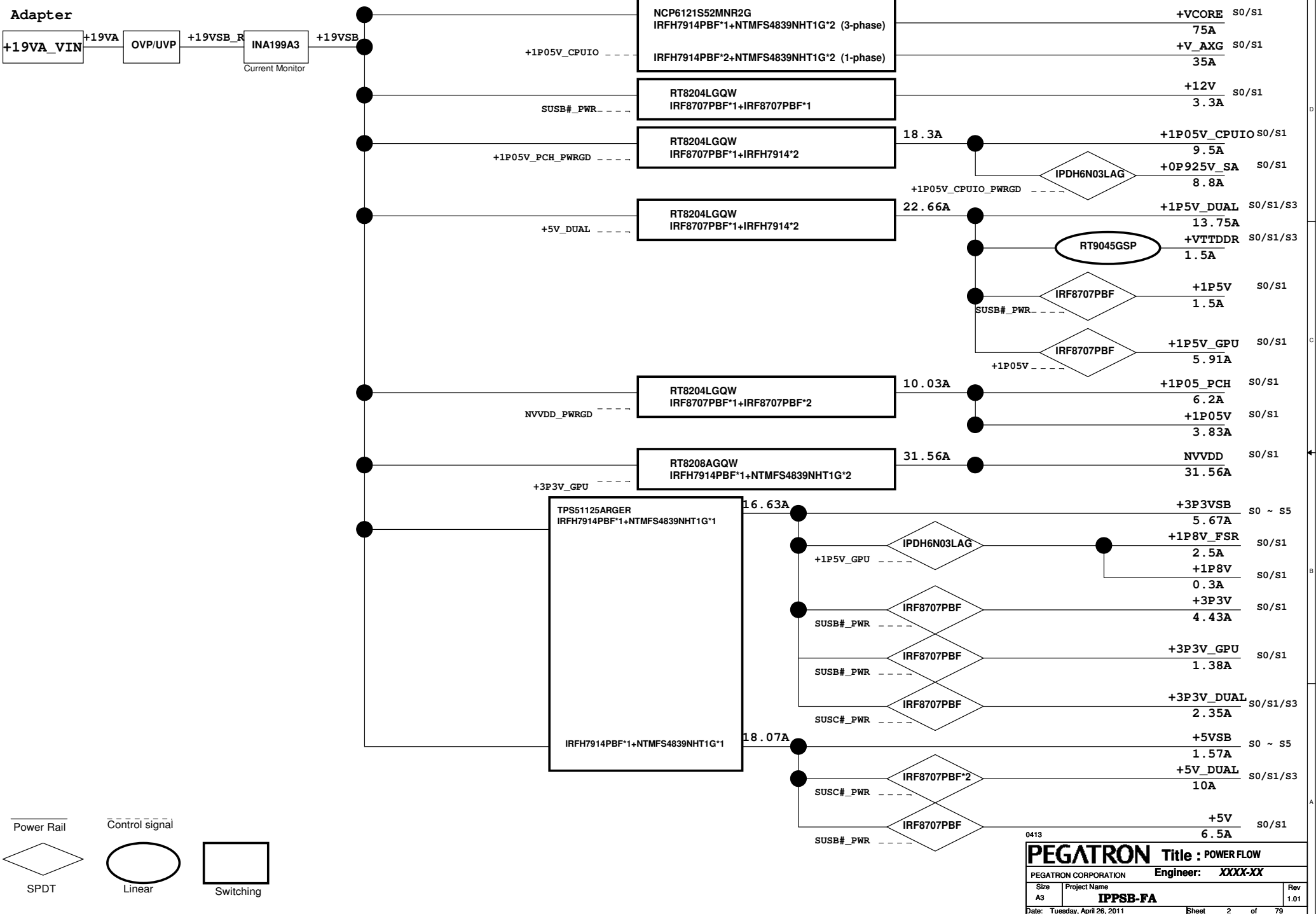
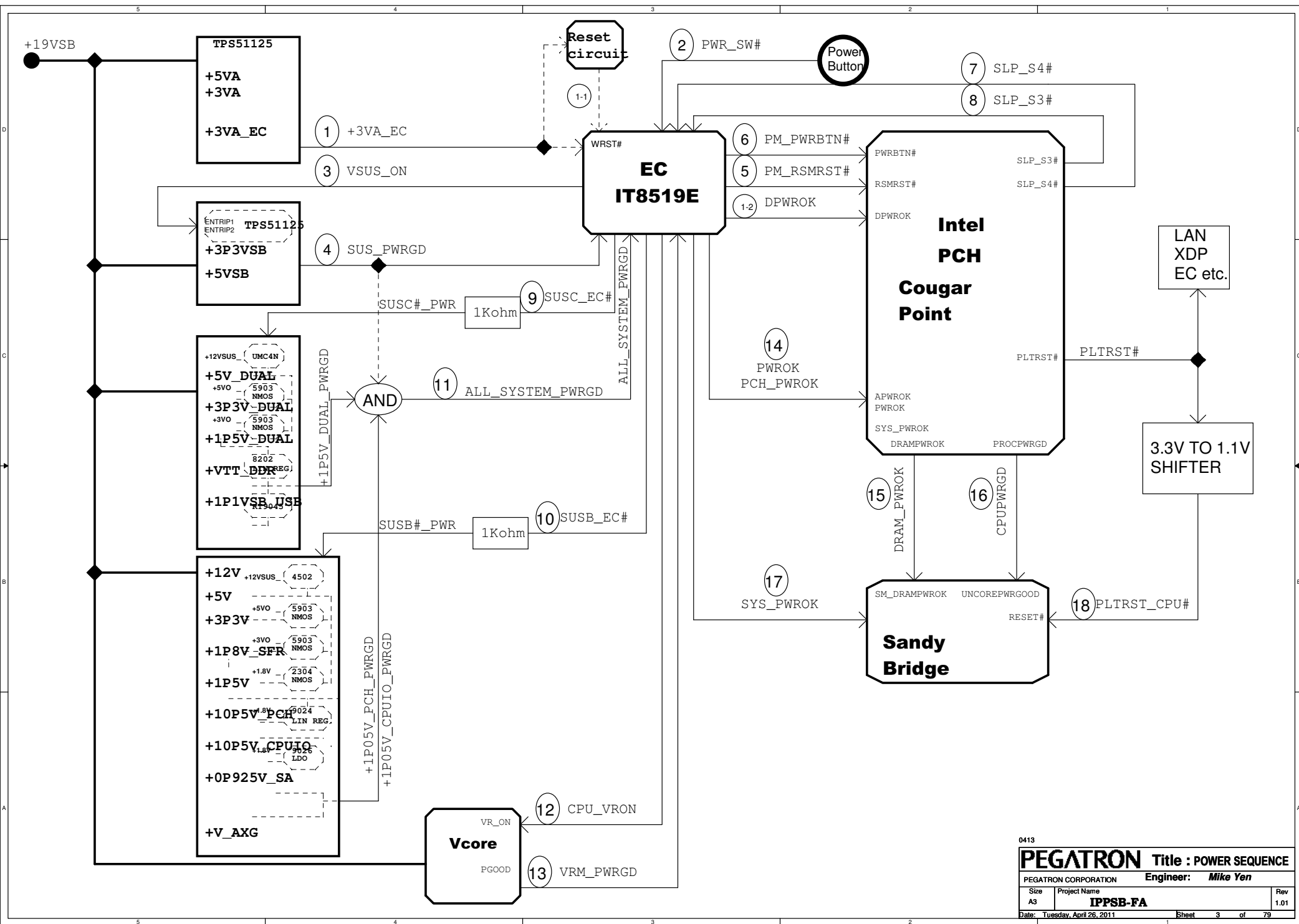


# IPPSB-FA

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02	POWER FLOW
03	POWER SEQUENCE
04~09	CPU LGA1155 DDR3 A 1-6
10	DDR3 CHANNEL A G/F
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52	+12V & +1P8V
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75	MXM.GPU Discharge
76	GPU_POWER&GND
77	MXM.NVVD
78	Card Reader RTS5139-GR
79	EDP CH7511

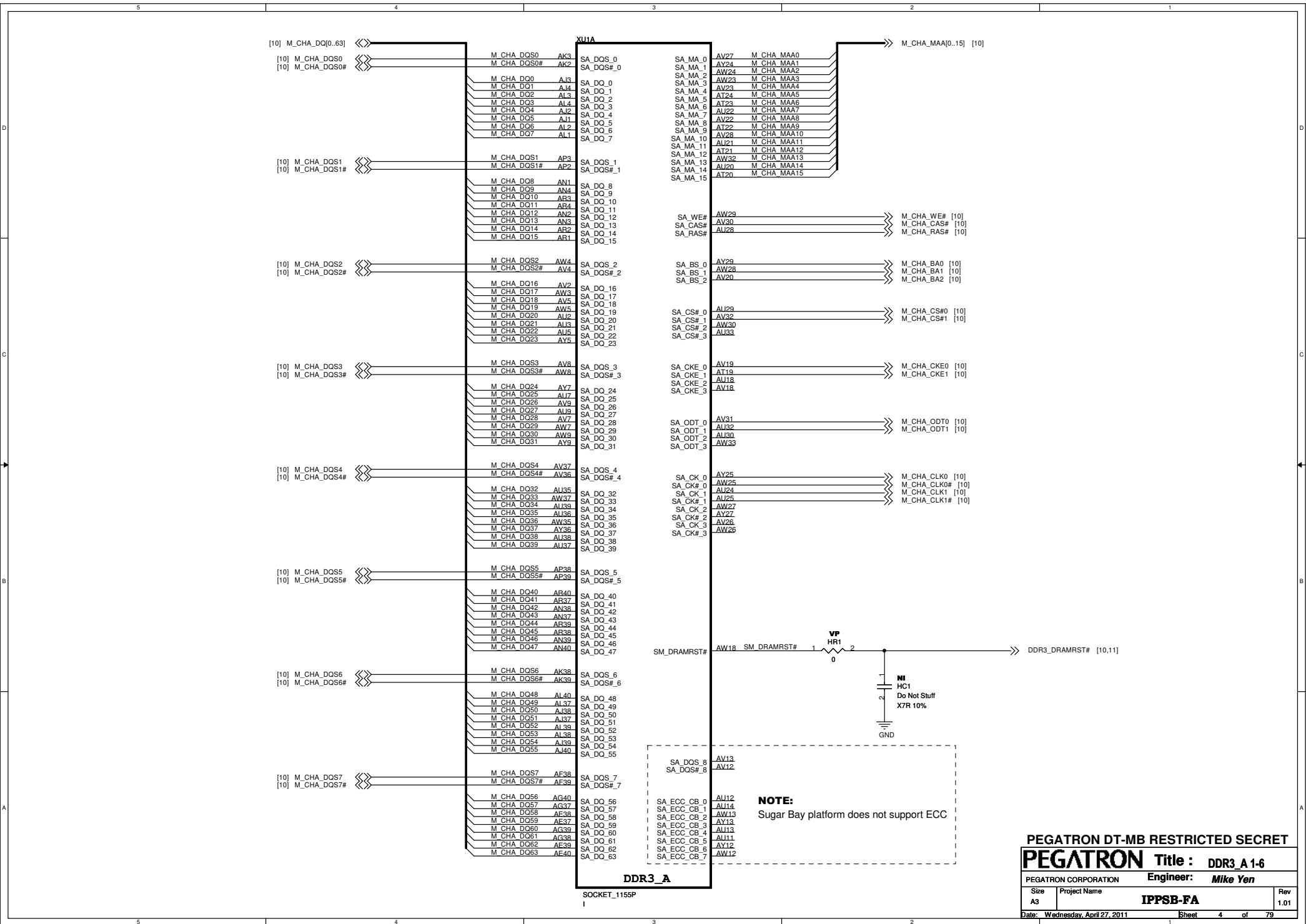






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PEGATRON		Title : POWER SEQUENCE	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Tuesday, April 26, 2011		Sheet 3 of 79	



PEGATRON DT-MB RESTRICTED SECRET

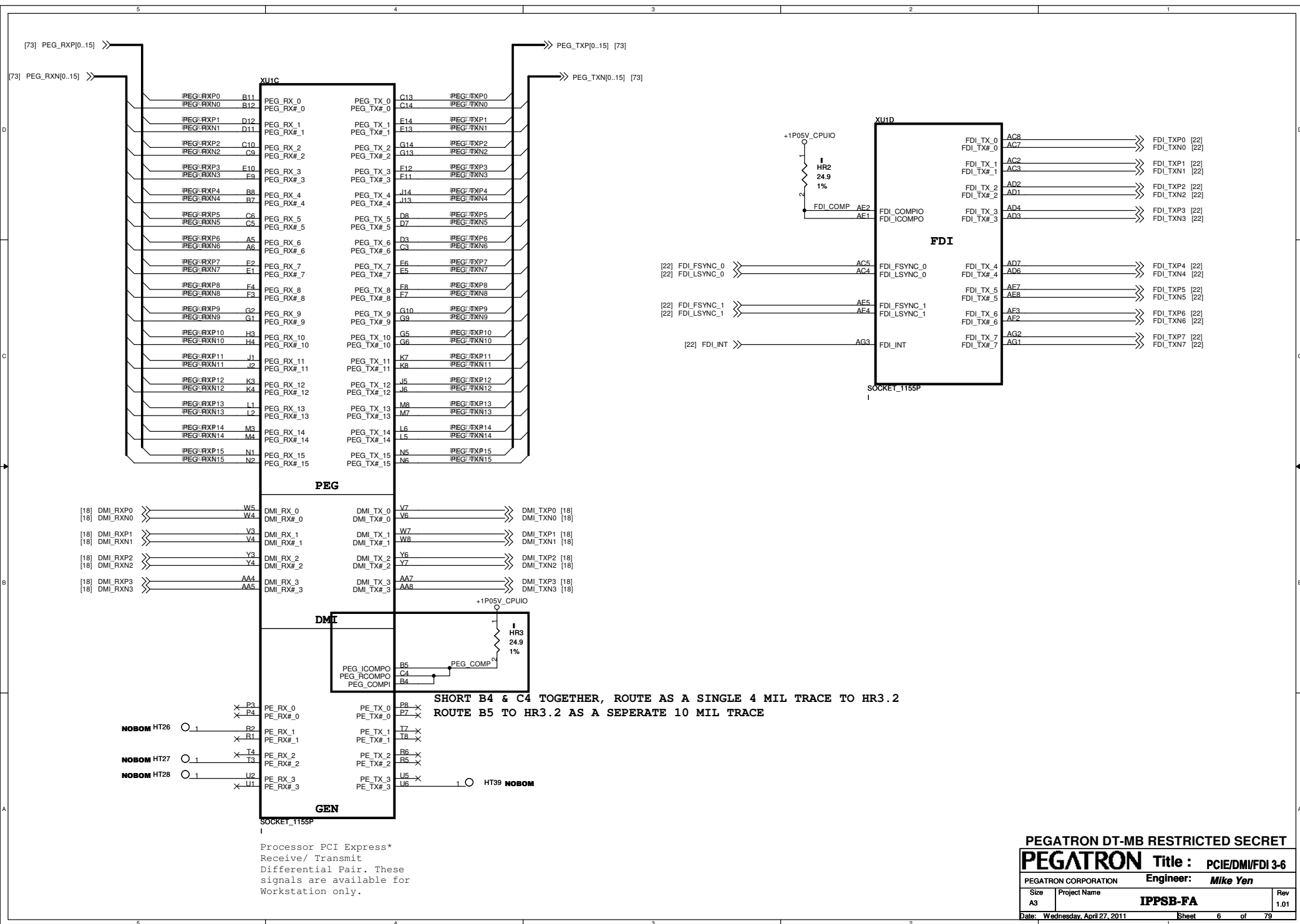
**PEGATRON** Title : DDR3\_A 1-6

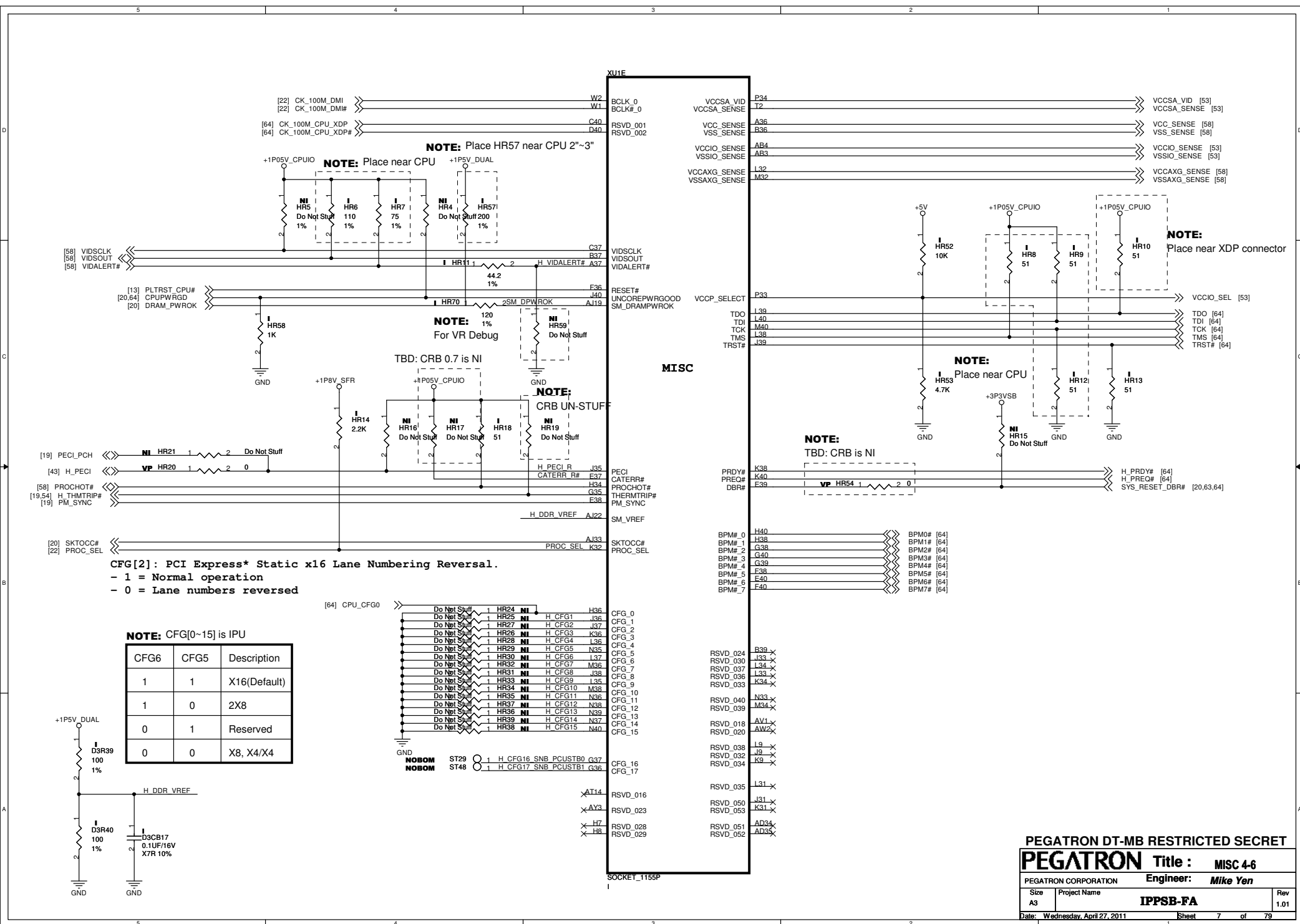
PEGATRON CORPORATION Engineer: Mike Yen

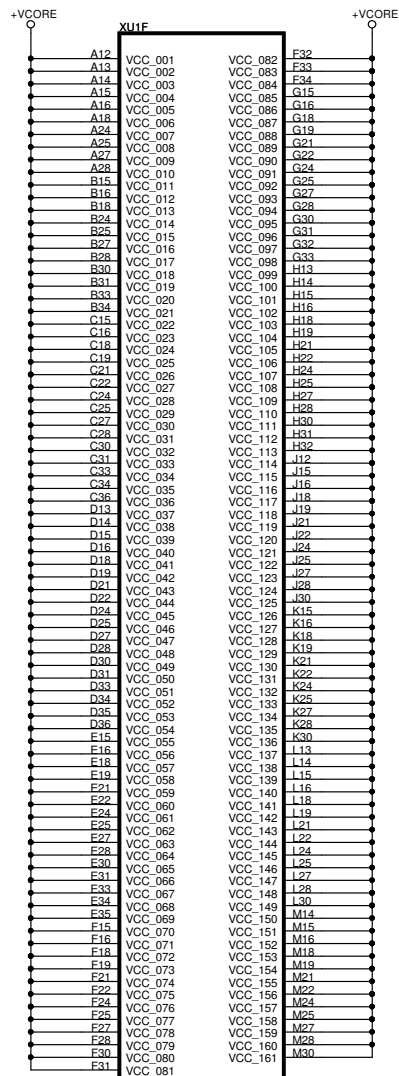
Size A3 Project Name IPPSB-FA Rev 1.01

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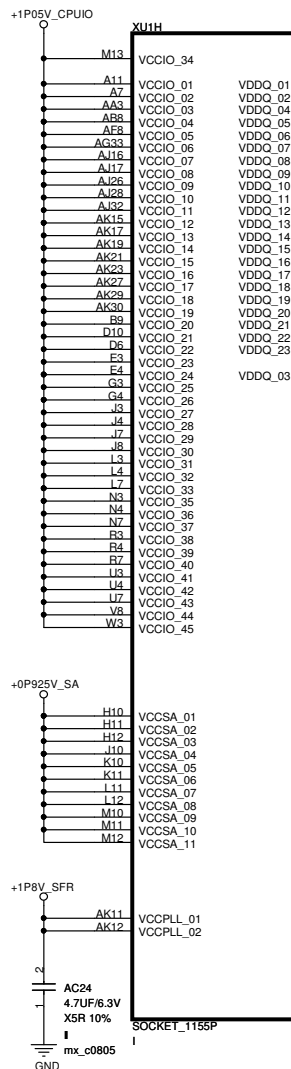






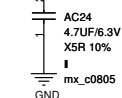


SOCKET\_1155P



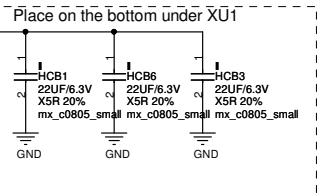
+0P925V\_SA

+1P8V\_SFR

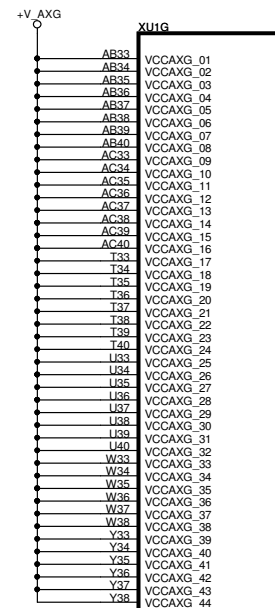


SOCKET\_1155P

+1P5V\_DUAL



Place on the bottom under XU1

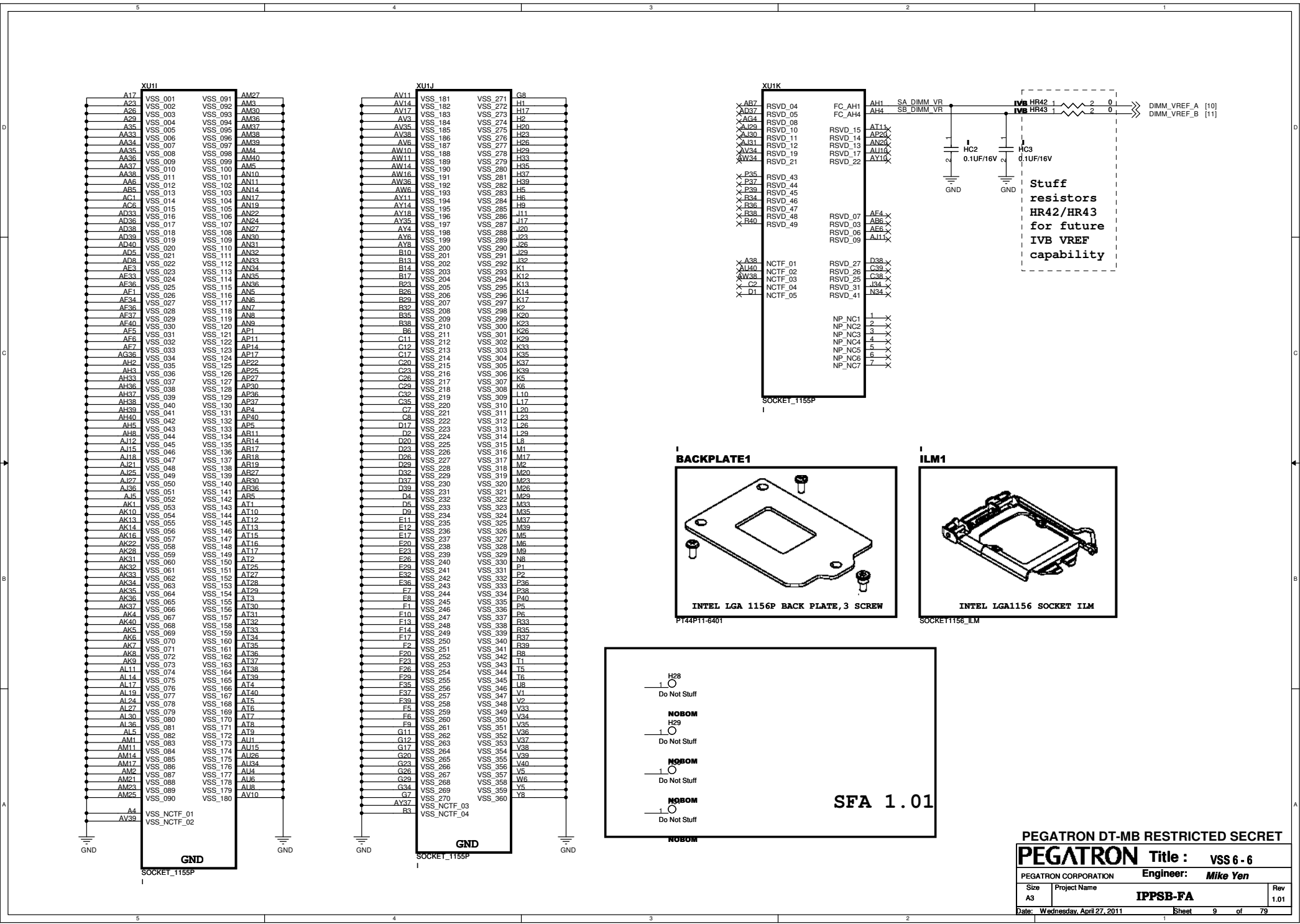


SOCKET\_1155P

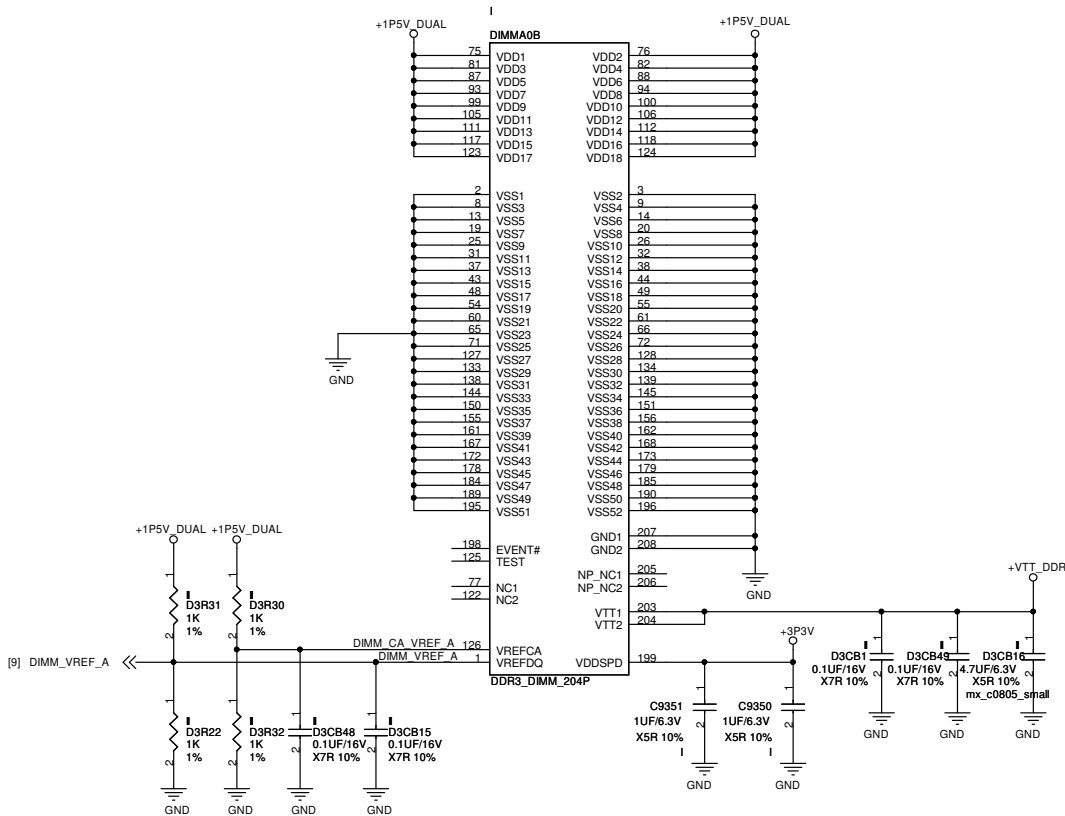
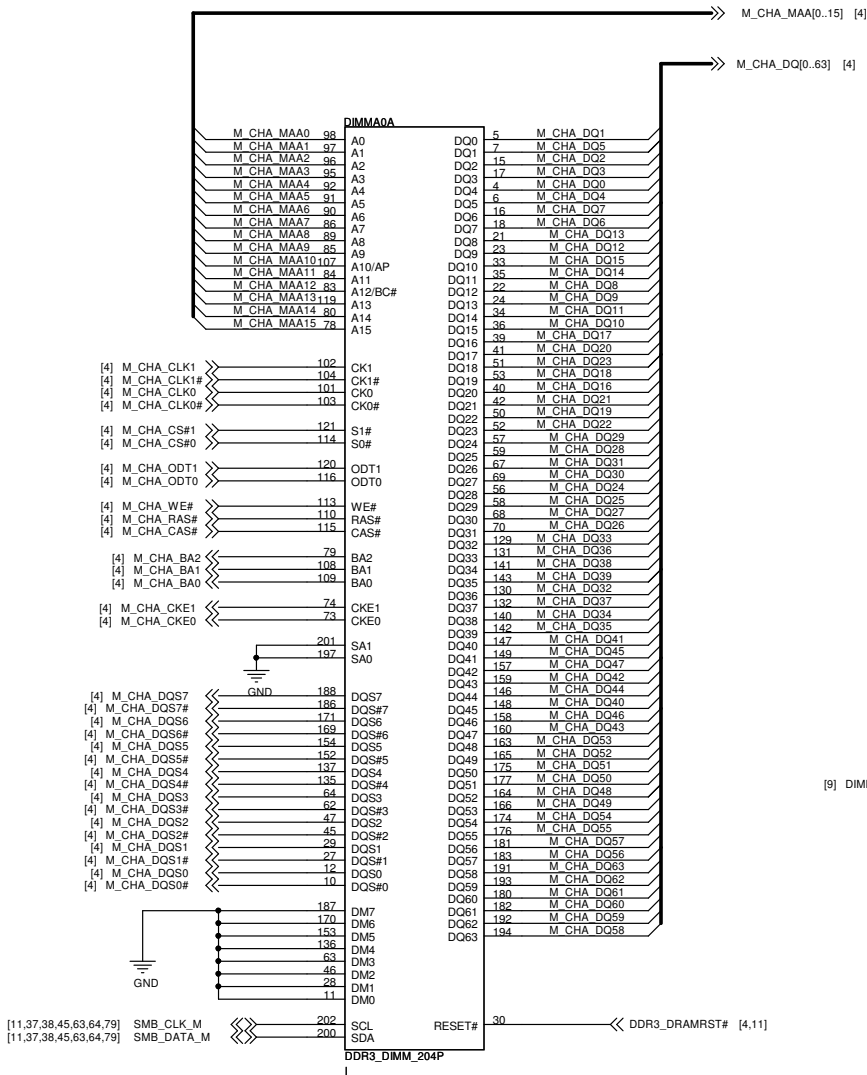
PEGATRON DT-MB RESTRICTED SECRET

<b>PEGATRON</b>		Title : VCC 5 - 6	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size A3	Project Name	IPPSB-FA	Rev 1.01
Date: Tuesday, April 26, 2011		Sheet 8	of 79





皆改爲5.2H



皆改爲5.2H

M\_CHB\_DQ[0..63] [5]

M\_CHB\_MAA[0..15] [5]

(5.2H)  
DIMMB0A

M_CHB_MAA0	88	A0	DQ0	5	M_CHB_DQ0
M_CHB_MAA1	87	A1	DQ1	7	M_CHB_DQ4
M_CHB_MAA2	86	A2	DQ2	15	M_CHB_DQ7
M_CHB_MAA3	85	A3	DQ3	17	M_CHB_DQ6
M_CHB_MAA4	92	A4	DQ4	4	M_CHB_DQ1
M_CHB_MAA5	91	A5	DQ5	6	M_CHB_DQ5
M_CHB_MAA6	90	A6	DQ6	16	M_CHB_DQ2
M_CHB_MAA7	86	A7	DQ7	18	M_CHB_DQ3
M_CHB_MAA8	89	A8	DQ8	21	M_CHB_DQ13
M_CHB_MAA9	85	A9	DQ9	23	M_CHB_DQ12
M_CHB_MAA10	107	A10/AP	DQ10	33	M_CHB_DQ15
M_CHB_MAA11	84	A11	DQ11	35	M_CHB_DQ14
M_CHB_MAA12	83	A12/BC#	DQ12	22	M_CHB_DQ8
M_CHB_MAA13	119	A13	DQ13	24	M_CHB_DQ9
M_CHB_MAA14	80	A14	DQ14	34	M_CHB_DQ10
M_CHB_MAA15	78	A15	DQ15	36	M_CHB_DQ11

[5] M\_CHB\_CLK1 >> 102 CK1  
[5] M\_CHB\_CLK1# >> 104 CK1#  
[5] M\_CHB\_CLK0 >> 101 CK0  
[5] M\_CHB\_CLK0# >> 103 CK0#

[5] M\_CHB\_CS#1 >> 121 S1#  
[5] M\_CHB\_CS#0 >> 114 S#

[5] M\_CHB\_ODT1 >> 120 ODT1  
[5] M\_CHB\_ODT0 >> 116 ODT0

[5] M\_CHB\_WE# >> 113 WE#  
[5] M\_CHB\_RAS# >> 110 RAS#  
[5] M\_CHB\_CAS# >> 115 CAS#

[5] M\_CHB\_BA2 << 79 BA2  
[5] M\_CHB\_BA1 << 108 BA1  
[5] M\_CHB\_BA0 << 109 BA0

[5] M\_CHB\_CKE1 << 74 CKE1  
[5] M\_CHB\_CKE0 << 73 CKE0

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

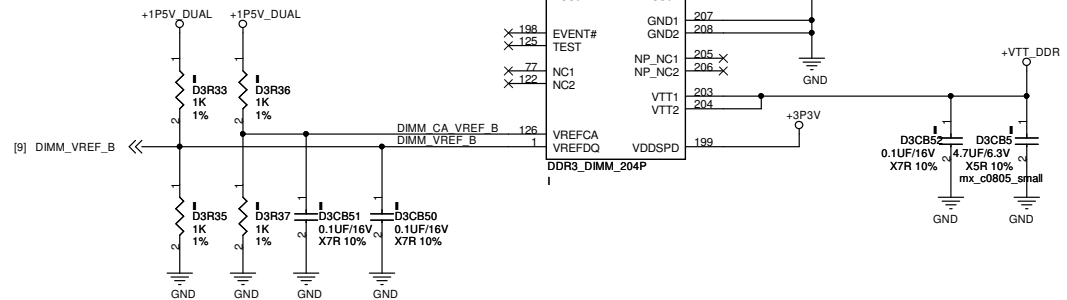
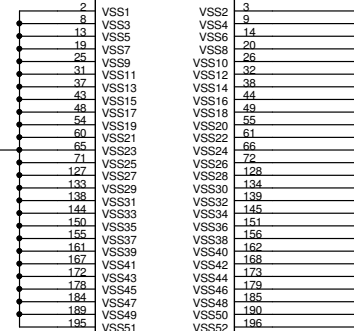
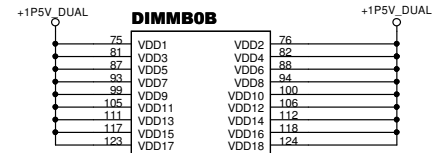
[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

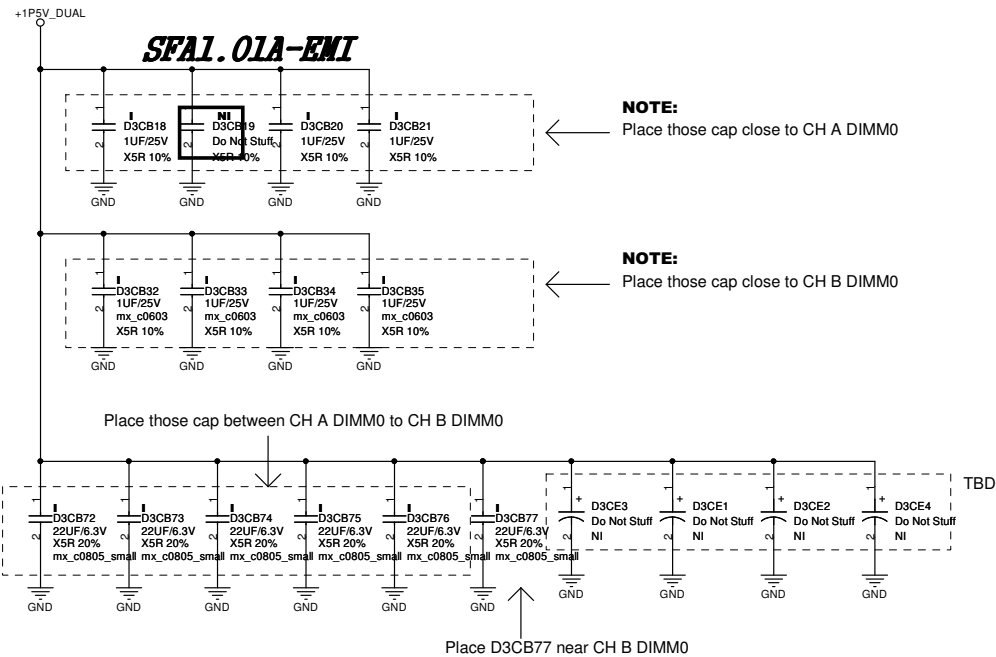
[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

[5] M\_CHB\_DQS7 << 188 DQS7  
[5] M\_CHB\_DQS7# << 186 DQS7#  
[5] M\_CHB\_DQS6 << 171 DQS6  
[5] M\_CHB\_DQS6# << 169 DQS6#  
[5] M\_CHB\_DQS5 << 154 DQS5  
[5] M\_CHB\_DQS5# << 152 DQS5#  
[5] M\_CHB\_DQS4 << 137 DQS4  
[5] M\_CHB\_DQS4# << 135 DQS4#  
[5] M\_CHB\_DQS3 << 64 DQS3  
[5] M\_CHB\_DQS3# << 62 DQS3#  
[5] M\_CHB\_DQS2 << 47 DQS2  
[5] M\_CHB\_DQS2# << 45 DQS2#  
[5] M\_CHB\_DQS1 << 29 DQS1  
[5] M\_CHB\_DQS1# << 27 DQS1#  
[5] M\_CHB\_DQS0 << 12 DQS0  
[5] M\_CHB\_DQS0# << 10 DQS0#

DQ0	5	M_CHB_DQ0
DQ1	7	M_CHB_DQ4
DQ2	15	M_CHB_DQ7
DQ3	17	M_CHB_DQ6
DQ4	4	M_CHB_DQ1
DQ5	6	M_CHB_DQ5
DQ6	16	M_CHB_DQ2
DQ7	18	M_CHB_DQ3
DQ8	21	M_CHB_DQ13
DQ9	23	M_CHB_DQ12
DQ10	33	M_CHB_DQ15
DQ11	35	M_CHB_DQ14
DQ12	22	M_CHB_DQ8
DQ13	24	M_CHB_DQ9
DQ14	34	M_CHB_DQ10
DQ15	36	M_CHB_DQ11
DQ16	39	M_CHB_DQ20
DQ17	41	M_CHB_DQ21
DQ18	51	M_CHB_DQ23
DQ19	53	M_CHB_DQ22
DQ20	49	M_CHB_DQ18
DQ21	42	M_CHB_DQ17
DQ22	50	M_CHB_DQ18
DQ23	52	M_CHB_DQ19
DQ24	57	M_CHB_DQ24
DQ25	59	M_CHB_DQ25
DQ26	67	M_CHB_DQ27
DQ27	69	M_CHB_DQ26
DQ28	56	M_CHB_DQ28
DQ29	58	M_CHB_DQ29
DQ30	68	M_CHB_DQ30
DQ31	70	M_CHB_DQ31
DQ32	129	M_CHB_DQ32
DQ33	131	M_CHB_DQ33
DQ34	141	M_CHB_DQ38
DQ35	143	M_CHB_DQ39
DQ36	130	M_CHB_DQ36
DQ37	132	M_CHB_DQ37
DQ38	140	M_CHB_DQ34
DQ39	142	M_CHB_DQ35
DQ40	147	M_CHB_DQ40
DQ41	149	M_CHB_DQ41
DQ42	157	M_CHB_DQ47
DQ43	159	M_CHB_DQ46
DQ44	146	M_CHB_DQ44
DQ45	148	M_CHB_DQ45
DQ46	158	M_CHB_DQ42
DQ47	160	M_CHB_DQ43
DQ48	163	M_CHB_DQ52
DQ49	165	M_CHB_DQ53
DQ50	177	M_CHB_DQ50
DQ51	164	M_CHB_DQ49
DQ52	174	M_CHB_DQ54
DQ53	176	M_CHB_DQ55
DQ54	181	M_CHB_DQ61
DQ55	183	M_CHB_DQ60
DQ56	181	M_CHB_DQ62
DQ57	183	M_CHB_DQ63
DQ58	180	M_CHB_DQ57
DQ59	182	M_CHB_DQ56
DQ60	192	M_CHB_DQ59
DQ61	194	M_CHB_DQ58
DQ62		
DQ63		

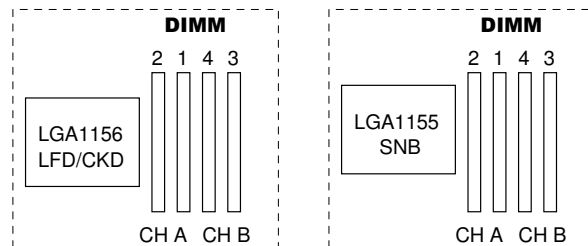
RESET# 30  
SCL 202  
SDA 200  
DDR3\_DIMM\_204P I  
D3C4 0.1UF/16V X7R 10%  
GND





**NOTE:**

**DIMM Placement for different platform**



PEGATRON DT-MB RESTRICTED SECRET

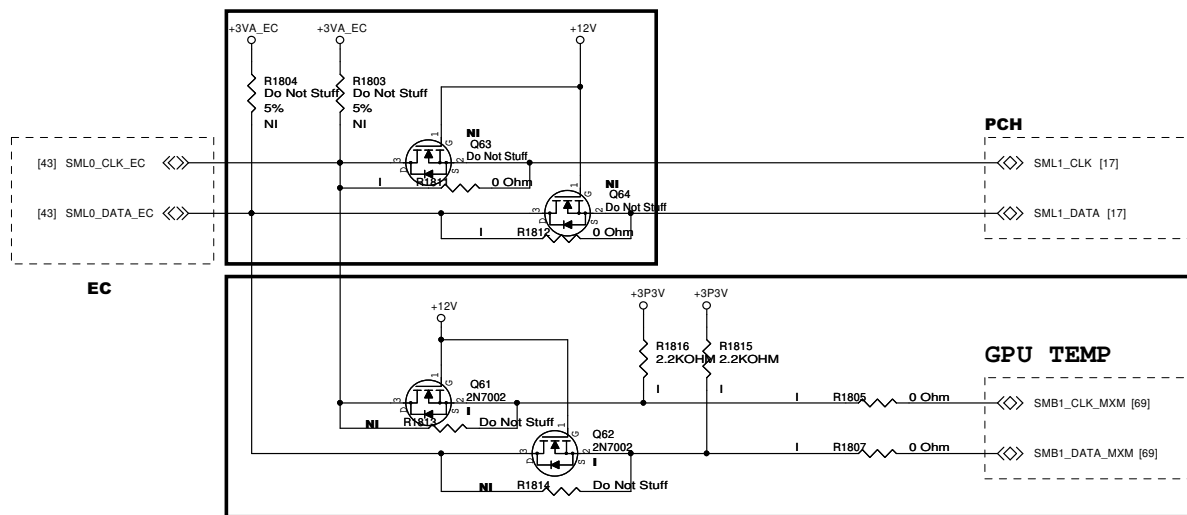
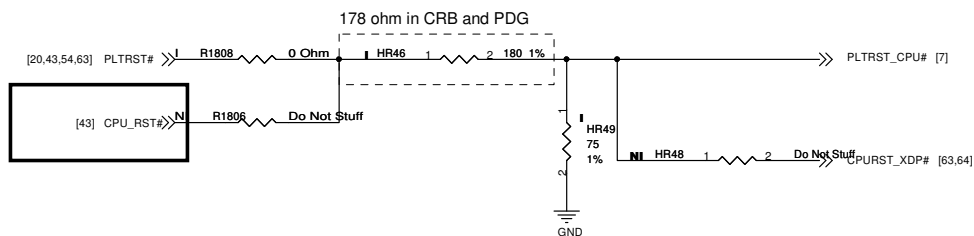
**PEGATRON** Title : DDR3 TERMINATION A&B

PEGATRON CORPORATION Engineer: **Mike Yen**

Size A3 Project Name **IPPSB-FA** Rev 1.01

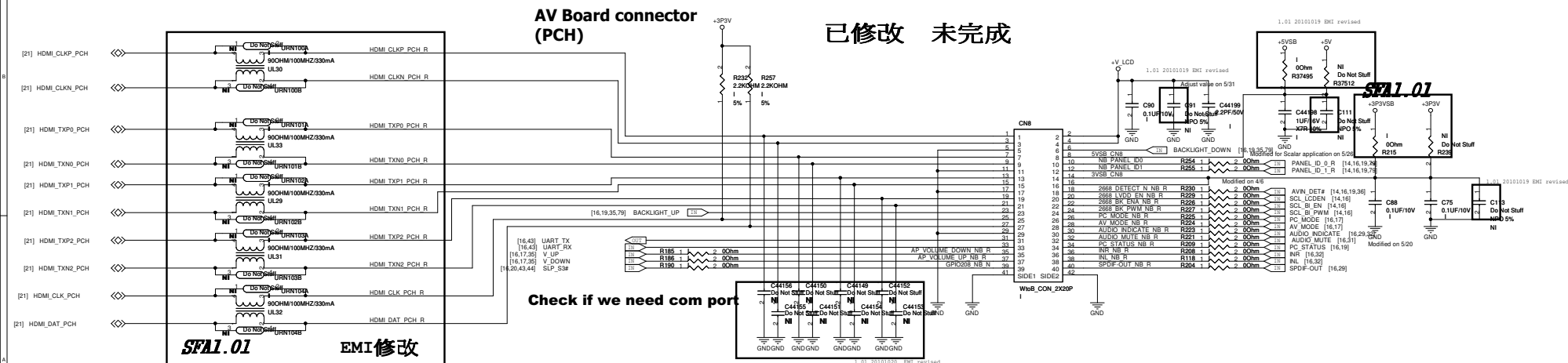
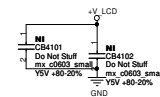
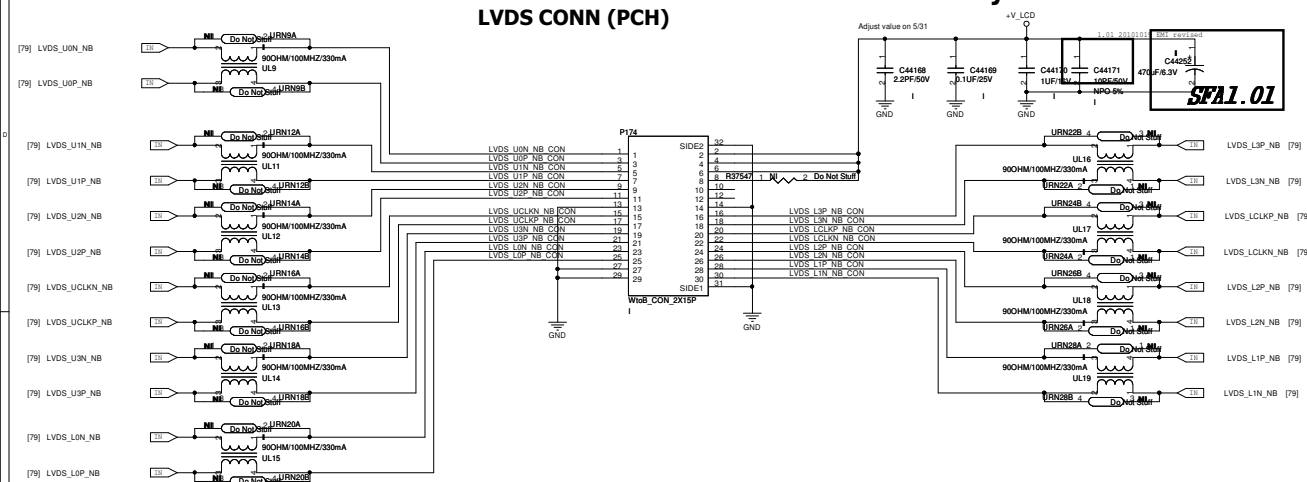
Date: Tuesday, April 26, 2011 Sheet 12 of 79

## PLTRST\_CPU#



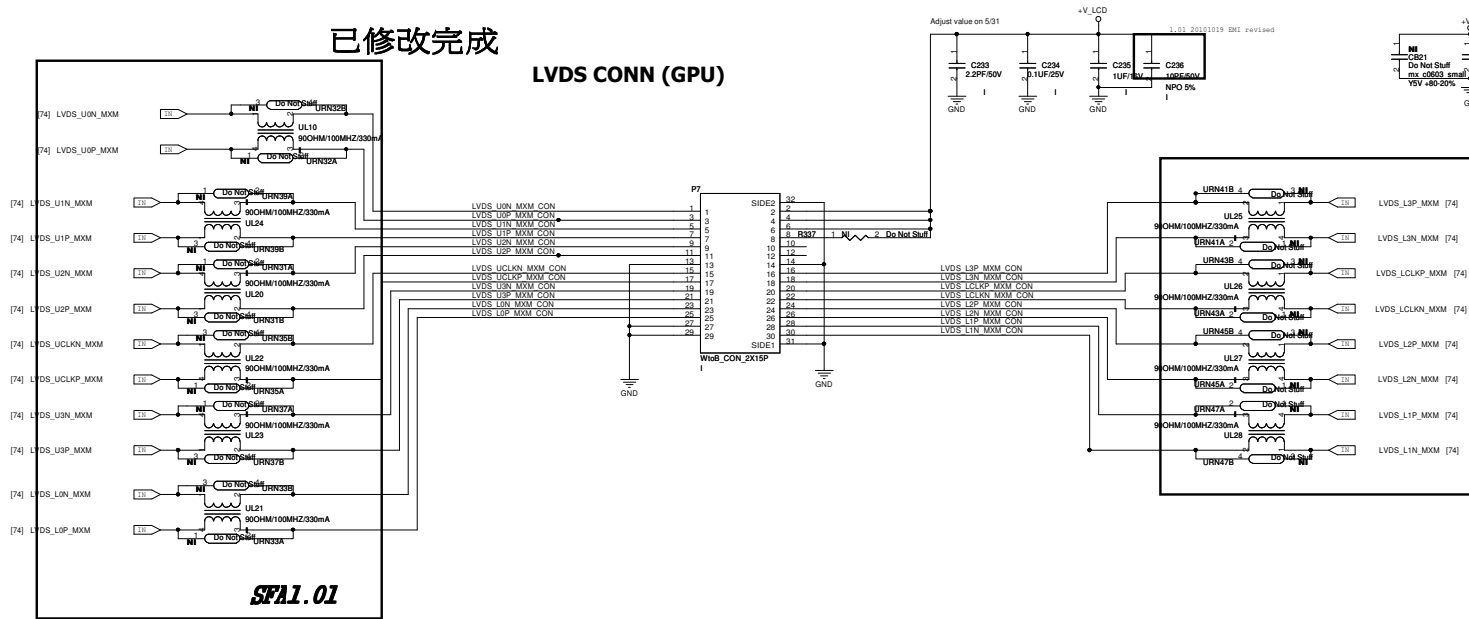


## LCD CONN NB & GPU colay



已修改完成

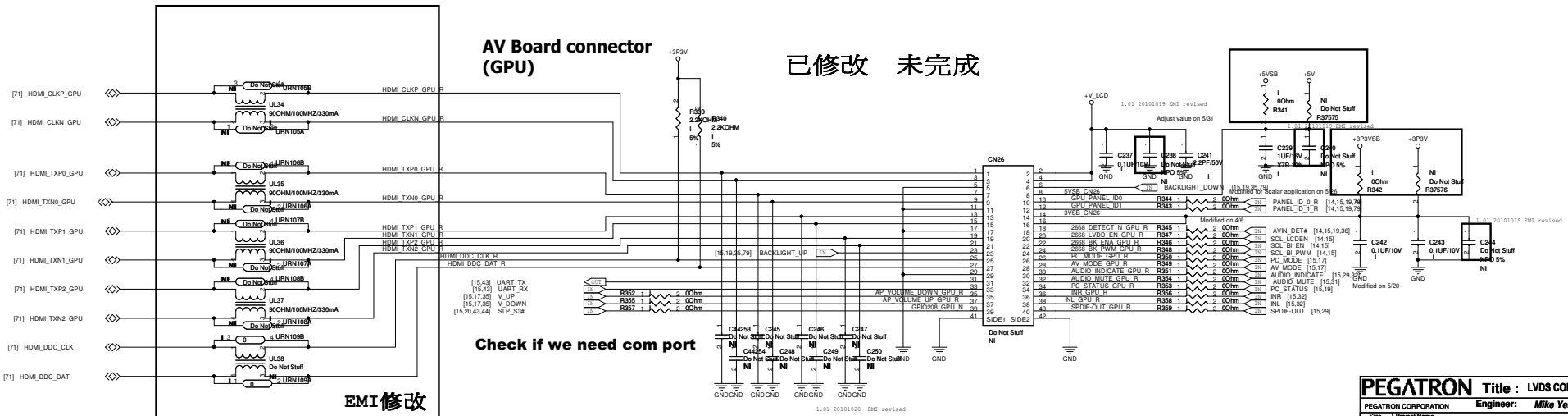
## LVDS CONN (GPU)



SA1.01

## AV Board connector (GPU)

已修改 未完成



Check if we need com port

EMI修改

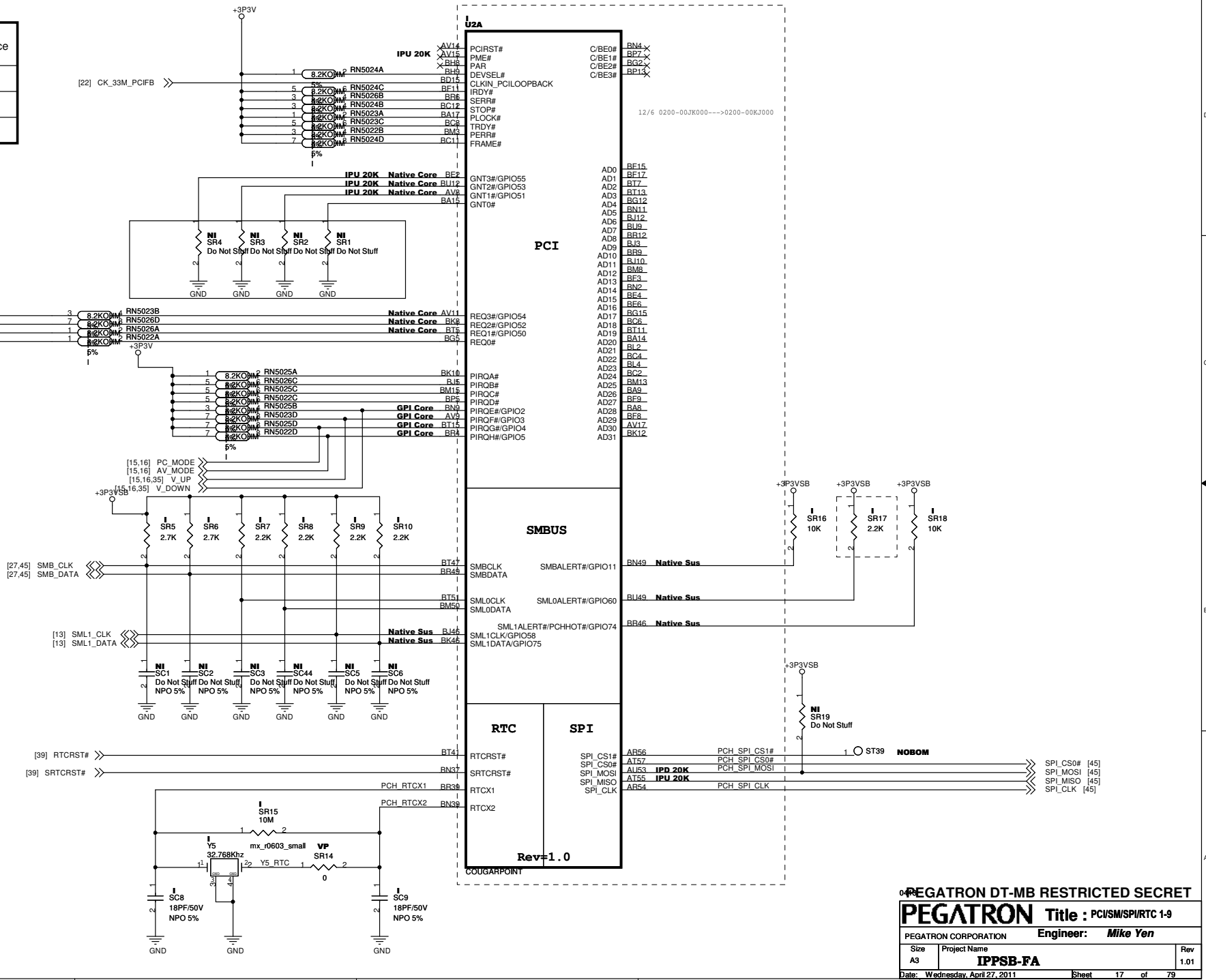
PEGATRON Title : LVDS CON			
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name	Rev	
A2	IPPSB-FA	1.01	
Date: Wednesday, April 27, 2011 Sheet 16 of 79			



**NOTE:** Strapping Options Flash

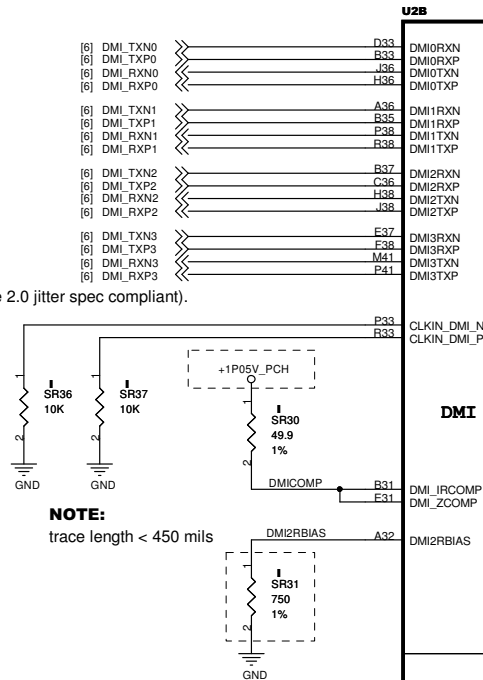
GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

I2C/en(dis)able/S3  
for accelerometer



**NOTE:**

Used for for DMI, PCIe(PCle 2.0 jitter spec compliant).



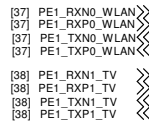
**NOTE:**

trace length < 450 mils

WLAN

TVT

LAN



for H61,  
PCIe ports 7 and 8 are disabled.

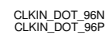
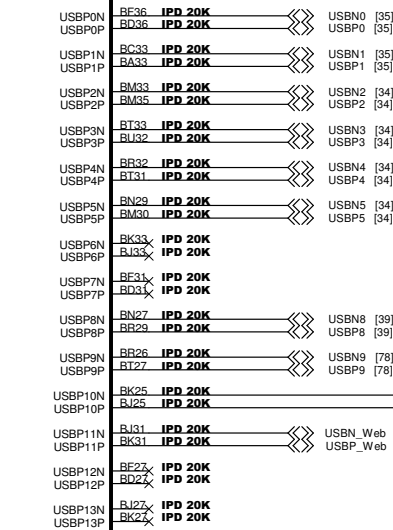
**U2B**

**DMI**

**PCIe**

**COUGARPOINT**

**USB**



side x2 #1 USB Debug port

Rear x4

Touch Panel

CARD READER #9 USB Debug port

Web Can

**NOTE:**

Used for integrated graphics, generate USB backbone,  
24MHz HDA bit, and 48MHz clock.

**NOTE:**

trace length < 200 mils

PEGATRON DT-MB RESTRICTED SECRET

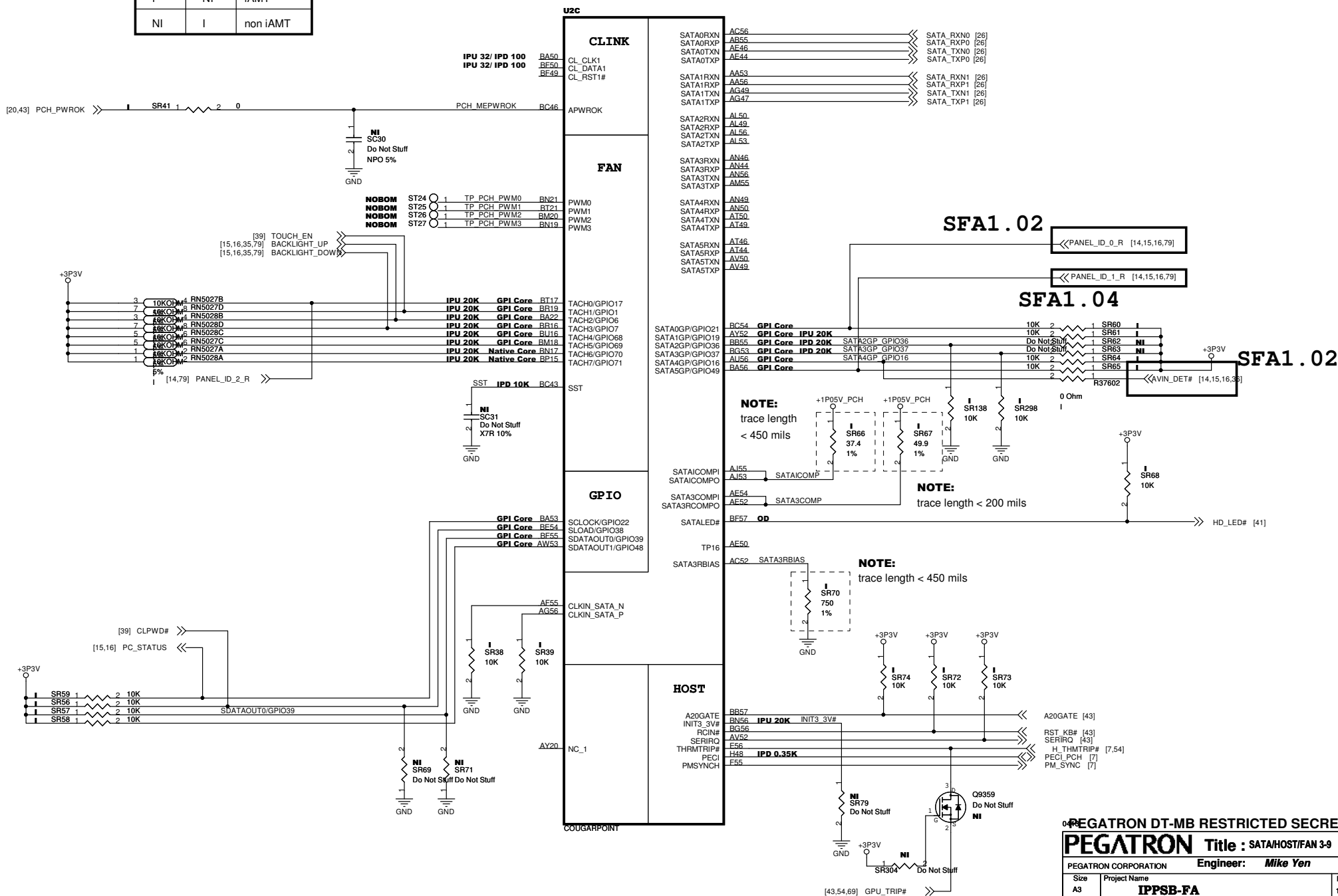
**PEGATRON** Title : PCIe/USB/DMI 2-9

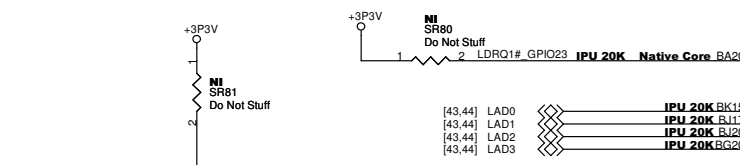
PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPPSB-FA Rev 1.01

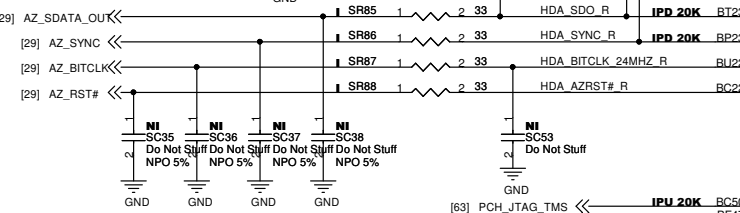
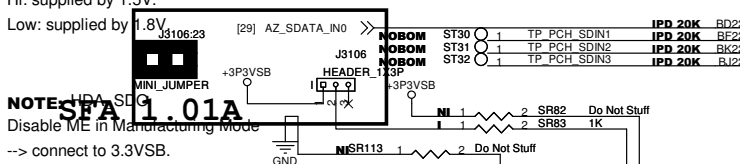
Date: Wednesday, April 27, 2011 Sheet 18 of 79

SR40	SR41	Description
I	NI	iAMT
NI	I	non iAMT

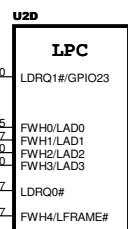
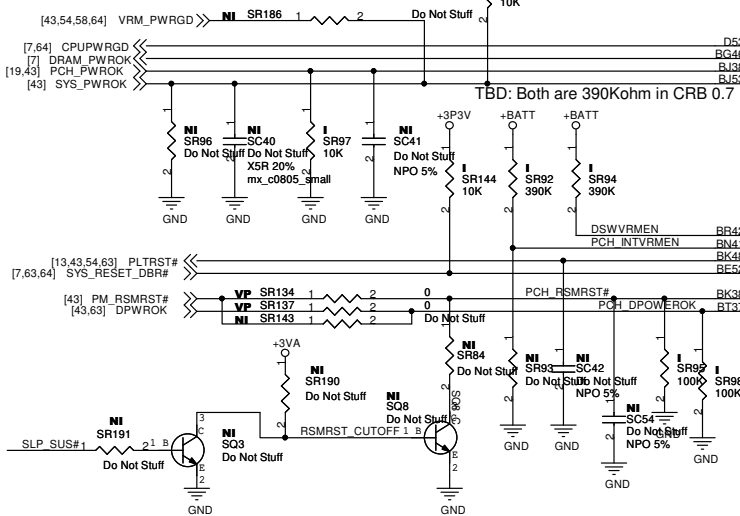




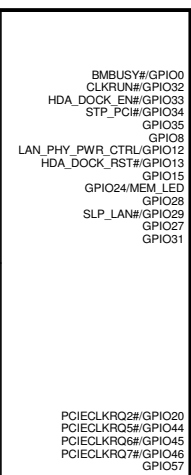
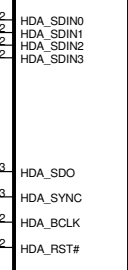
**NOTE:** HDA\_SYNC  
On-die PLL VR voltage selector.  
Hi: supplied by 1.5V.  
Low: supplied by 1.8V.



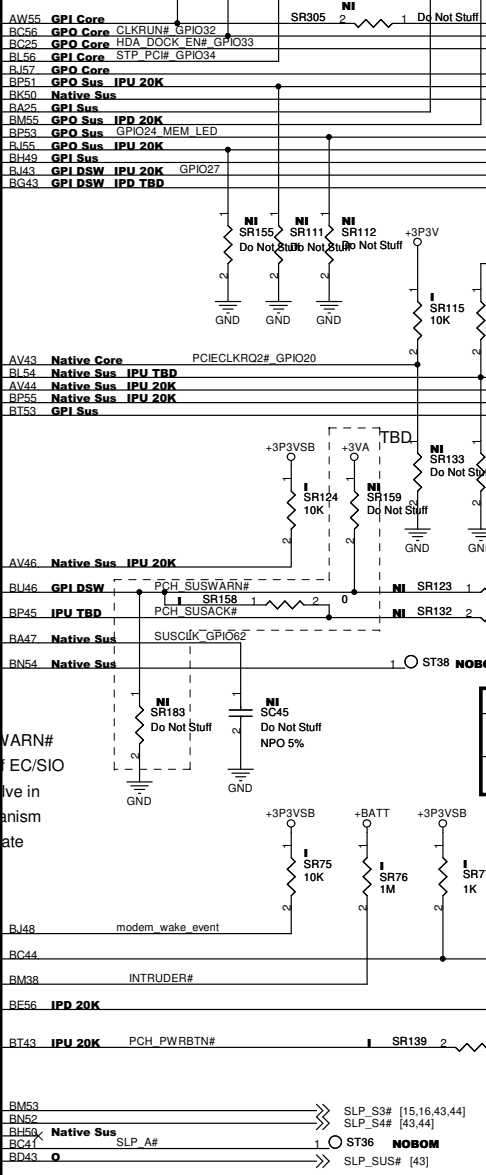
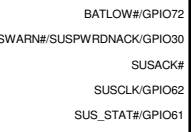
**NOTE:** CRB 0.7 is 1.1K ohm with 1%  
For platform not supporting deep sleep connect directly to RSMRST#.  
The DSW rails must be stable for at least 10 ms before DPWR0K is asserted to PCH.



### AUDIO



**NOTE:** SUSACK# and SUSWARN# can be tied together if EC/SIO does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.



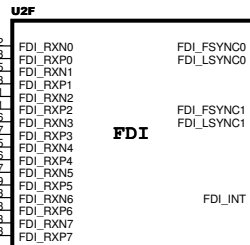
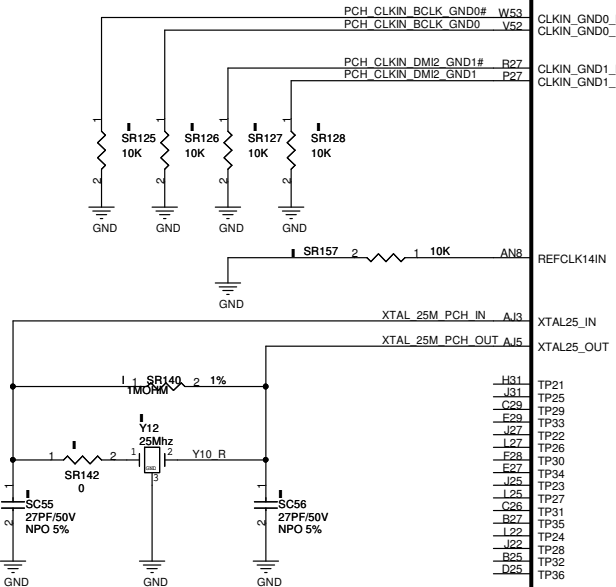
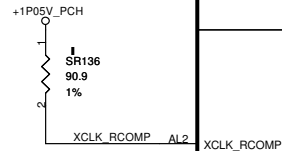
PIN	HIGH	LOW	DESCRIPTION
GPIO15	Enable	Disable	TLS confidentiality
GPIO28	Enable	Disable	On-Die PLL VR





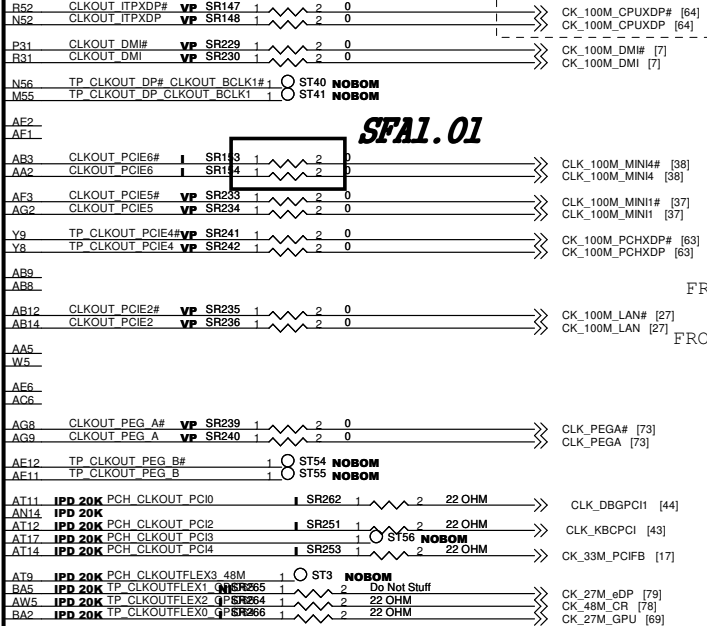
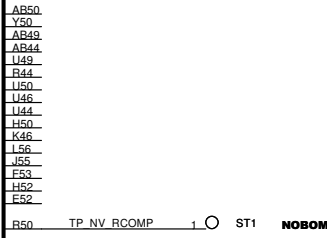
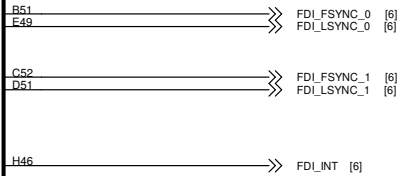
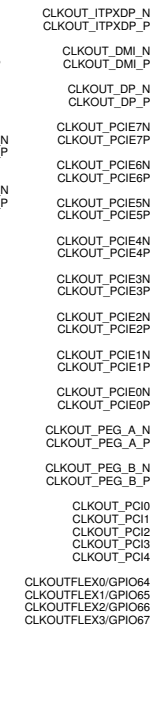
[7] PROC\_SEL >>> HR23 2 1 4.7K DF TVS IPD 20K M48 B47 Y41 M50 M49 M43 J57 Reserved\_001 Reserved\_002 Reserved\_003 Reserved\_004 Reserved\_005 Reserved\_006 Reserved\_007 Reserved\_008 Reserved\_009 Reserved\_010 Reserved\_011 Reserved\_012

Place HR23 close to NVRAM connector and minimize this stub to <100 mils with PCH and NVRAM connector



## RSD

## CLOCK

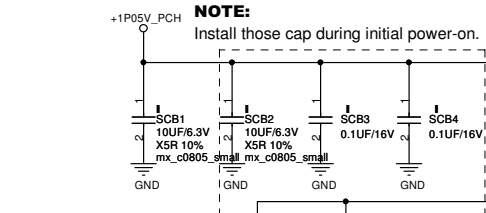


## NOTE:

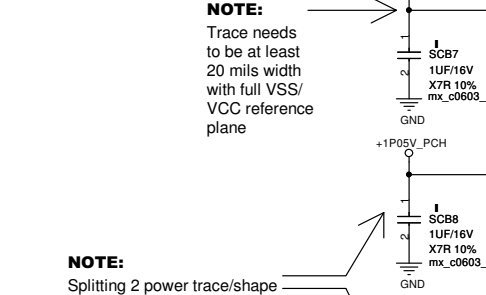
1. Prioritize 27/14/24/48/25-MHz FLEX on FLEX1/3.
2. Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0/2 if more than 2 PCI clocks + PCI loopback are routed.
3. With 2 PCI clocks routed (or less), prioritize the FLEX clocks to FLEX1/3 a. 27MHz(SSC/non-SSC) b. 14.31818MHz c. 24/48 d. 25MHz

PEGATRON DT-MB RESTRICTED SECRET

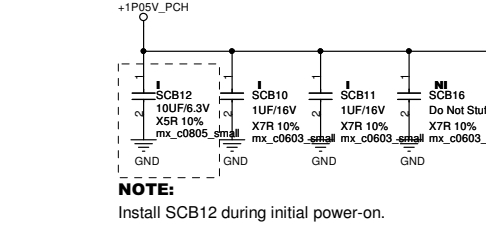
<b>PEGATRON</b>		<b>Title : CLK/NVRAM/FDI 6-9</b>	
PEGATRON CORPORATION		<b>Engineer: Mike Yen</b>	
Size A3	Project Name <b>IPPSB-FA</b>		Rev 1.01
Date: Wednesday, April 27, 2011		Sheet 22	of 79



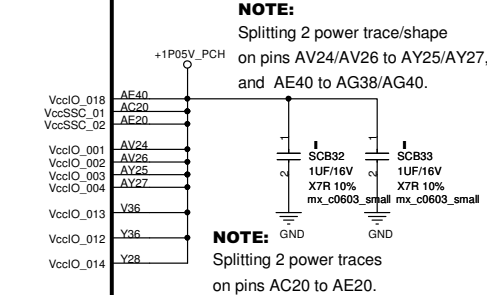
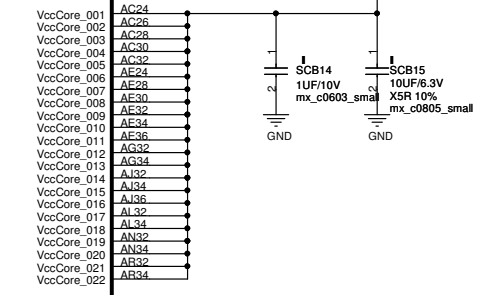
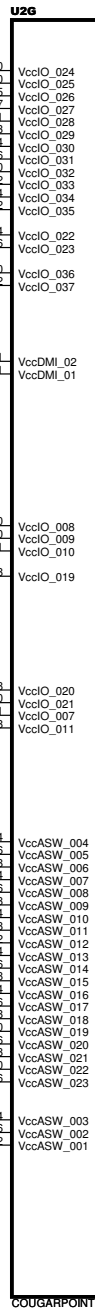
**NOTE:**  
Splitting 2 power trace/shape  
on pin Y20/Y22/V22 to other pins



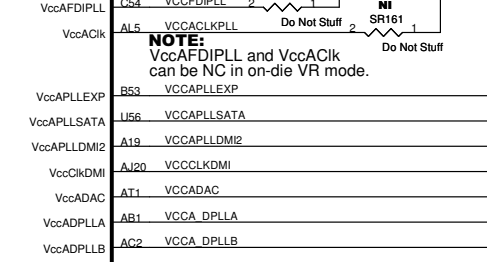
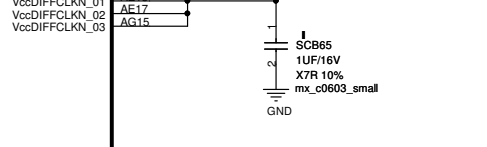
**NOTE:**  
Splitting 2 power trace/shape



**NOTE:**  
Install SCB12 during initial power-on.

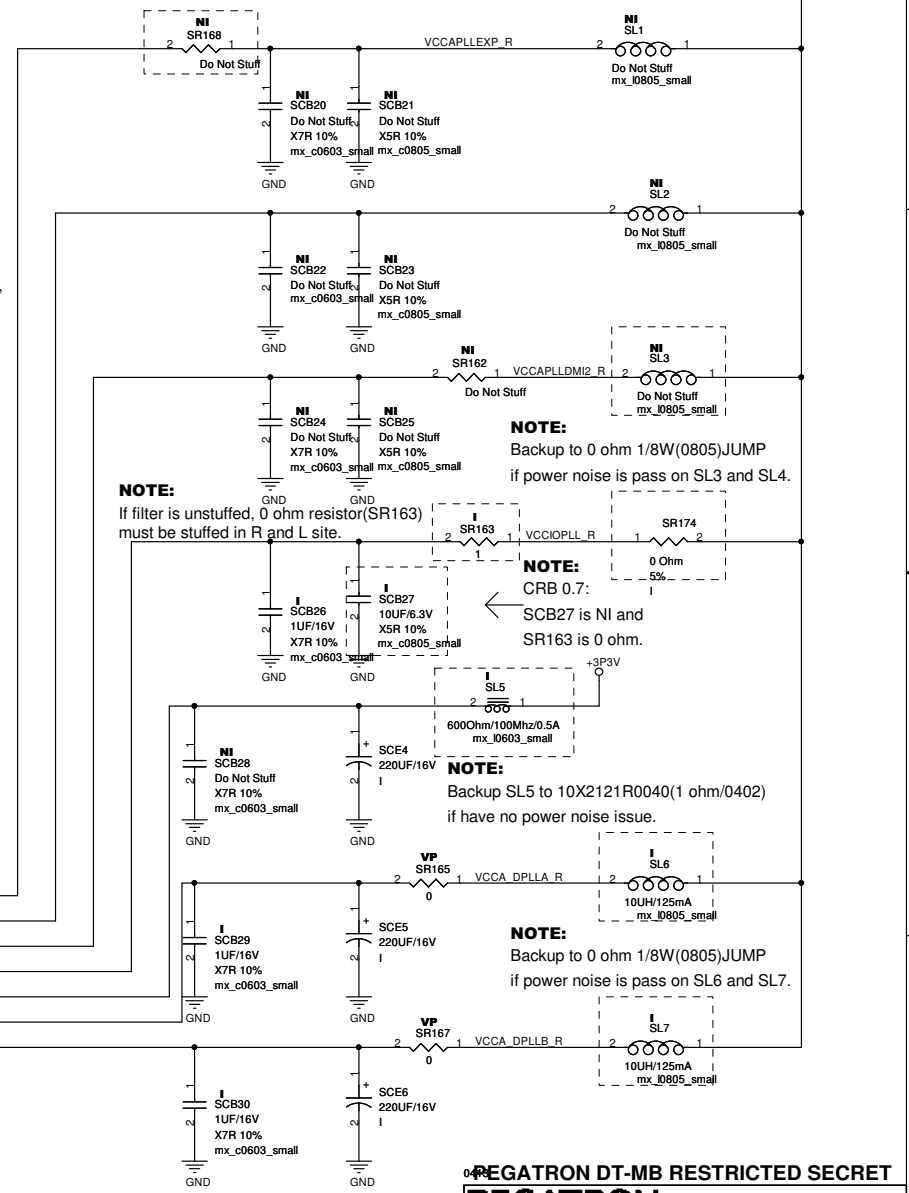


**NOTE:**  
Splitting 2 power traces  
on pins AC20 to AE20.



**NOTE:**  
VccAFDIPLL and VccACIK  
can be NC in on-die VR mode.

**NOTE:**  
VccAPLLEXP, VccAPLLSATA, and VccAPLLDMI2 can be NC  
in On-Die VR mode.



**NOTE:**  
If filter is unstuffed, 0 ohm resistor (SR163)  
must be stuffed in R and L site.

**NOTE:**  
Backup to 0 ohm 1/8W(0805)JUMP  
if power noise is pass on SL3 and SL4.

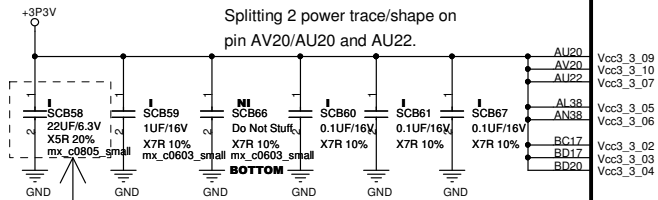
**NOTE:**  
CRB 0.7:  
SCB27 is NI and  
SR163 is 0 ohm.

**NOTE:**  
Backup SL5 to 10X2121R0040(1 ohm/0402)  
if have no power noise issue.

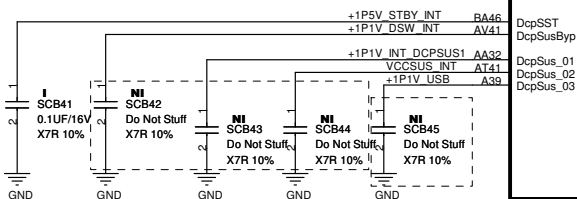
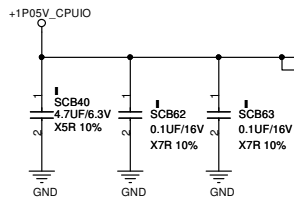
**NOTE:**  
Backup to 0 ohm 1/8W(0805)JUMP  
if power noise is pass on SL6 and SL7.

**NOTE:**  
Place SCB59 and SCB66 near pin AU20,  
SCB60 near pin AL38,  
SCB61 and SCB67 near BC17.

**NOTE:**  
Splitting 2 power trace/shape on  
pin AV20/AU20 and AU22.

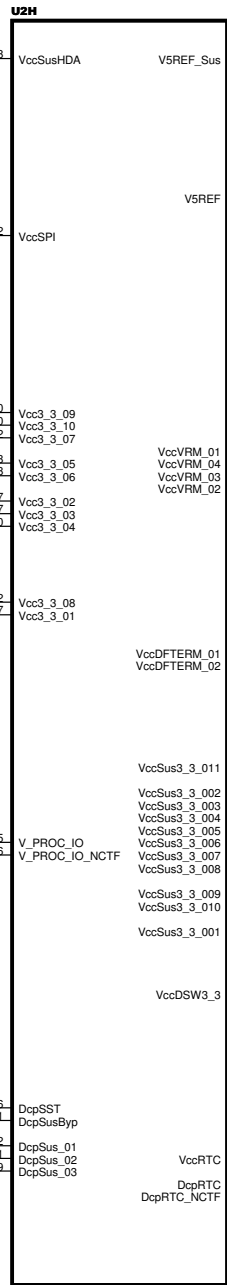


**NOTE:**  
Install SCB58 during initial power-on.

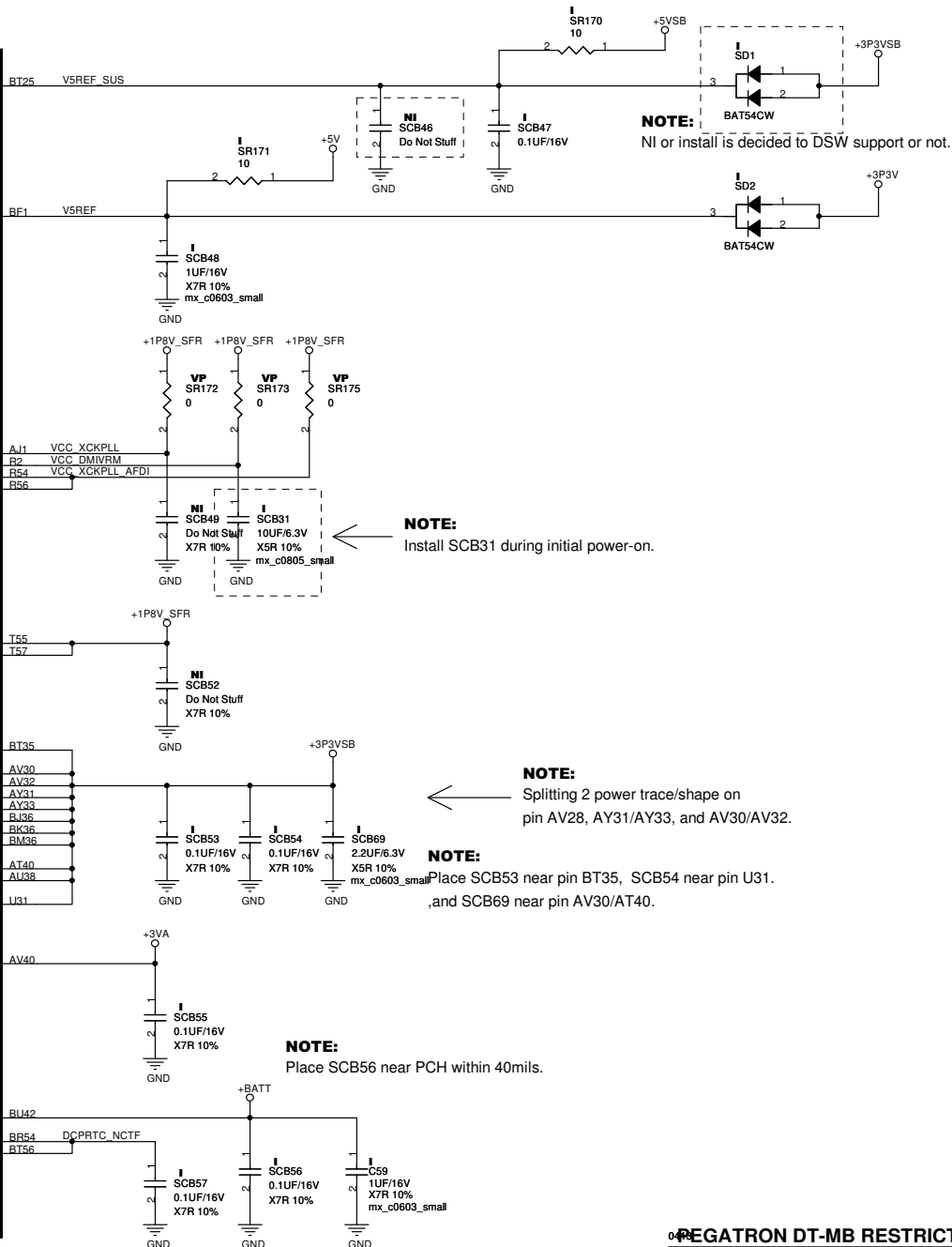


**NOTE:**  
Just for measurement.

CRB 0.7 is 1uF



COUGARPOINT



**NOTE:**  
NI or install is decided to DSW support or not.

**NOTE:**  
Install SCB31 during initial power-on.

**NOTE:**  
Splitting 2 power trace/shape on  
pin AV28, AY31/AY33, and AV30/AV32.

**NOTE:**  
Place SCB53 near pin BT35, SCB54 near pin U31,  
and SCB69 near pin AV30/AT40.

**NOTE:**  
Place SCB56 near PCH within 40mils.

PEGATRON DT-MB RESTRICTED SECRET

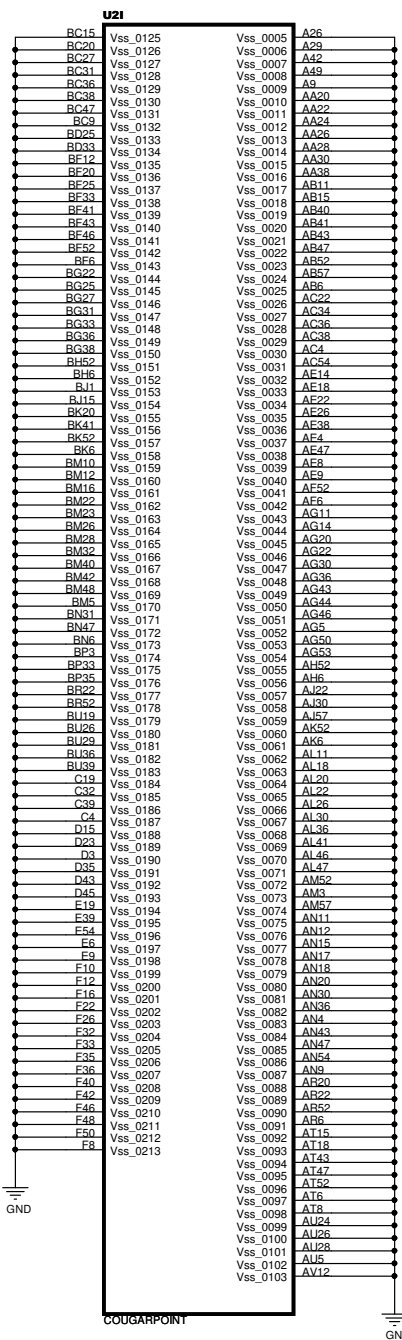
**PEGATRON** Title : VCCSUS 8-9

PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPPSB-FA Rev 1.01

Date: Tuesday, April 26, 2011 Sheet 24 of 79

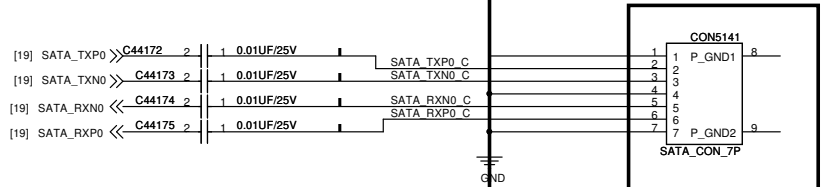




已更改完成

### SATA HDD CON

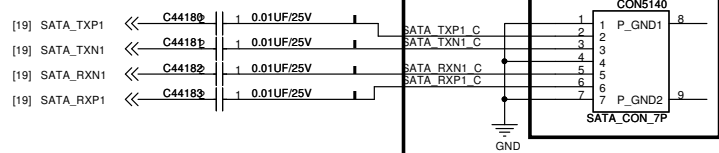
1.01 20101019 revised



**SATA CONTROLLER #1  
(MASTER)  
COLOR = DARK BLUE**

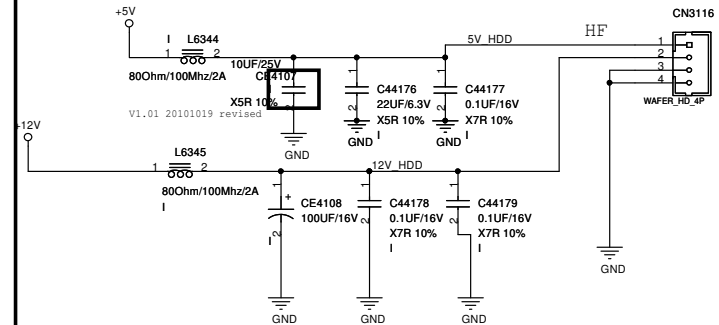
### SATA ODD CON

1.01 20101019 revised

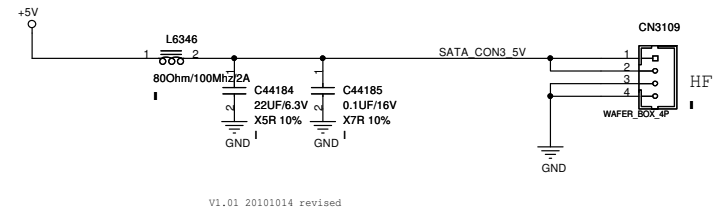


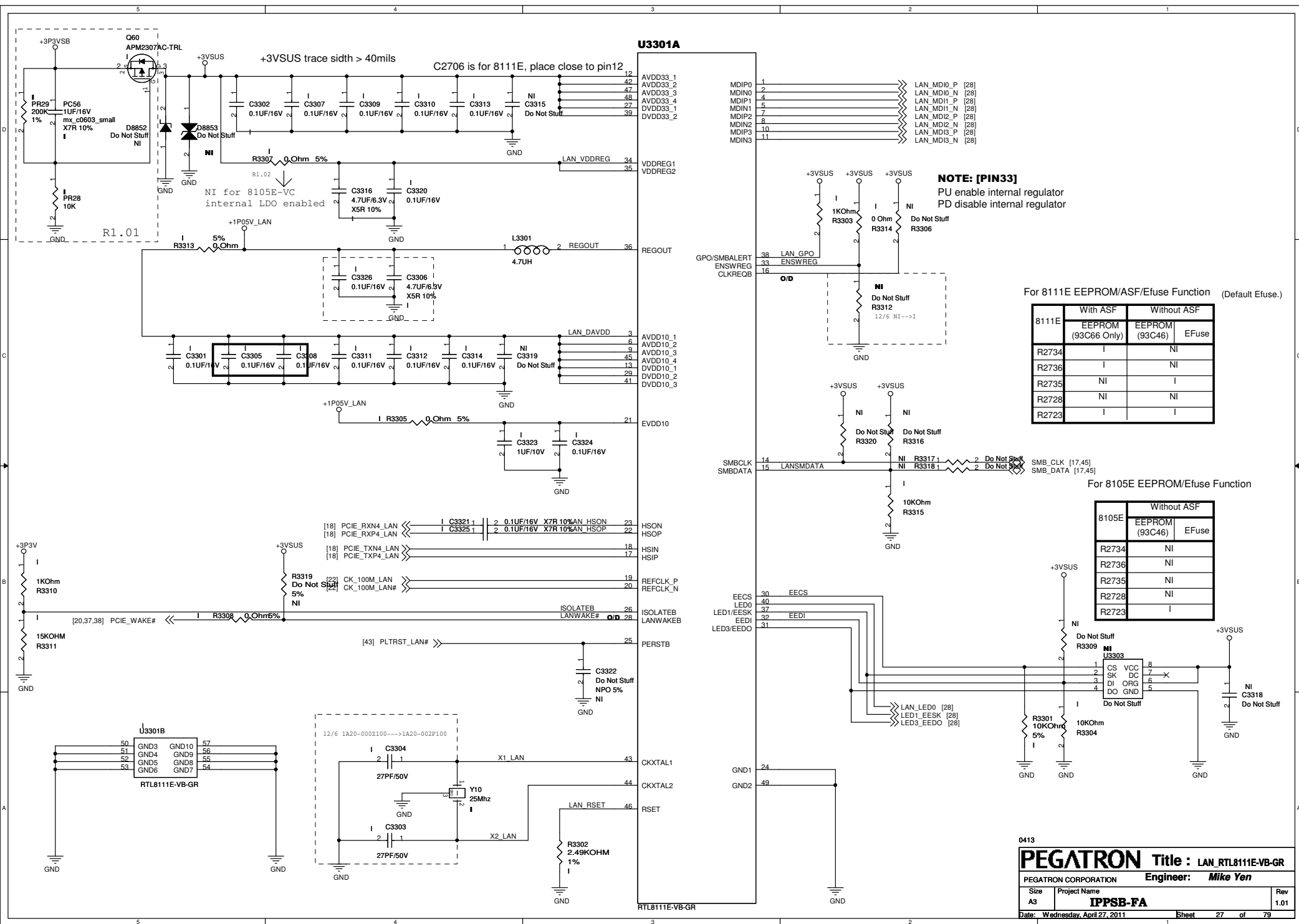
**SATA CONTROLLER #2  
(SLAVE)  
COLOR = WHITE**

### SATA POWER CONN.

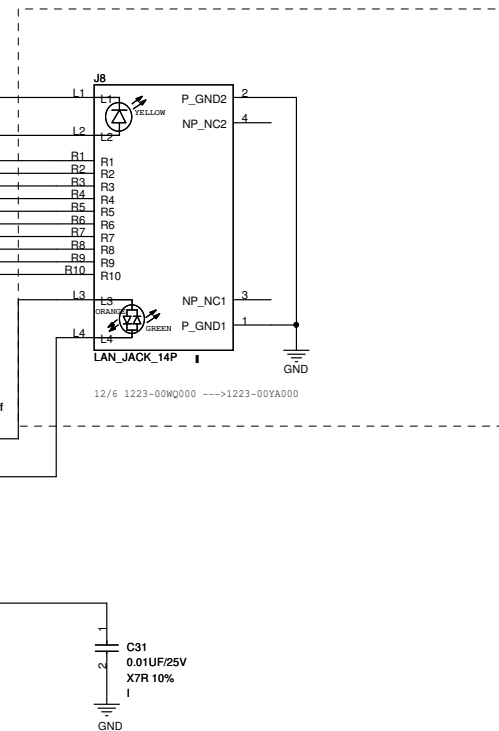
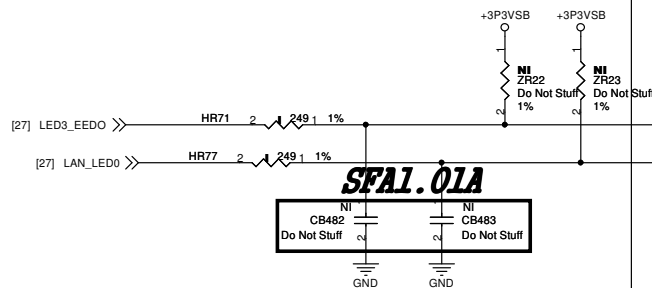
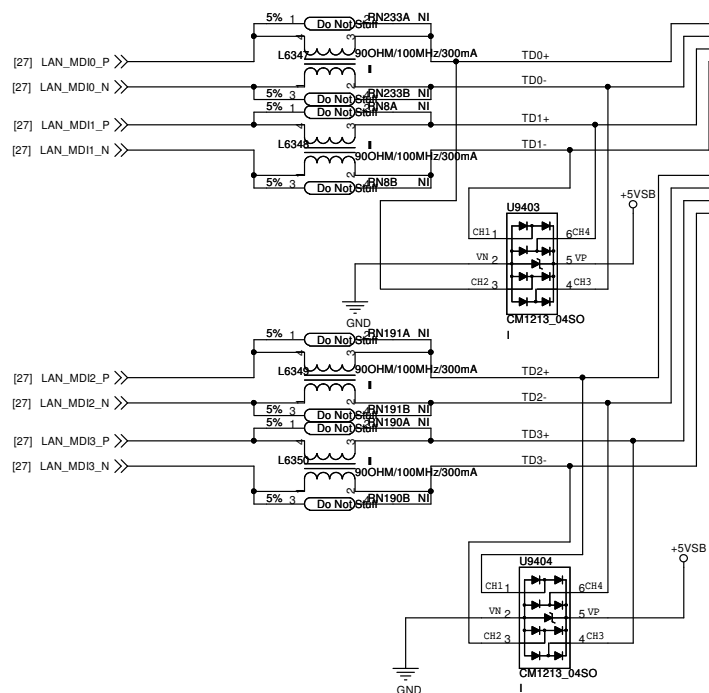
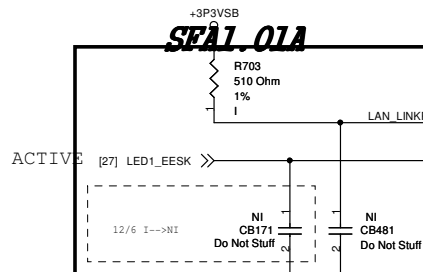


### ODD POWER CONN.



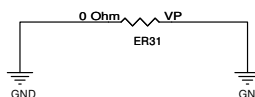


+3P3VSB  
**SEA1 01A**



**SFA1.OLA**

State	LINK Green LED	Yellow LED ACTIVE
S0	ON	OFF or blinking
S1,S3,S4	OFF	OFF



Next to PIN38

Next to PIN25

SFA 1.01A

vc版本上

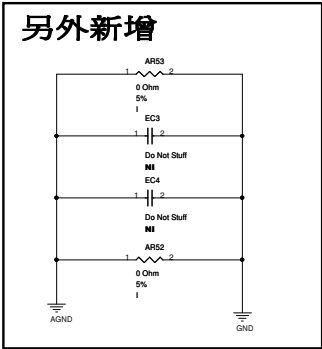
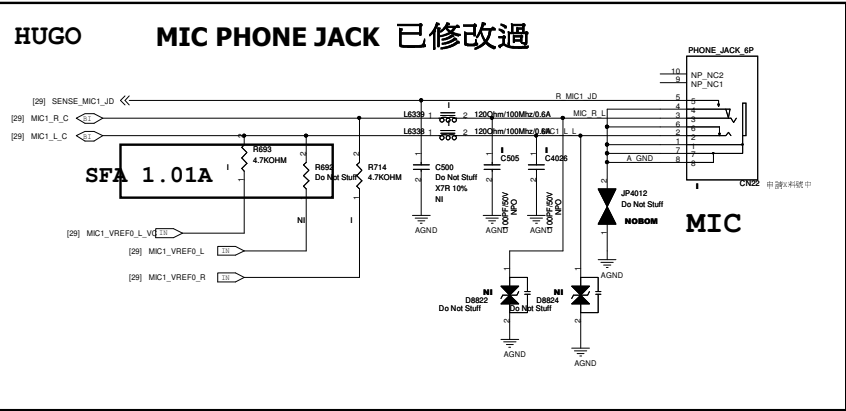
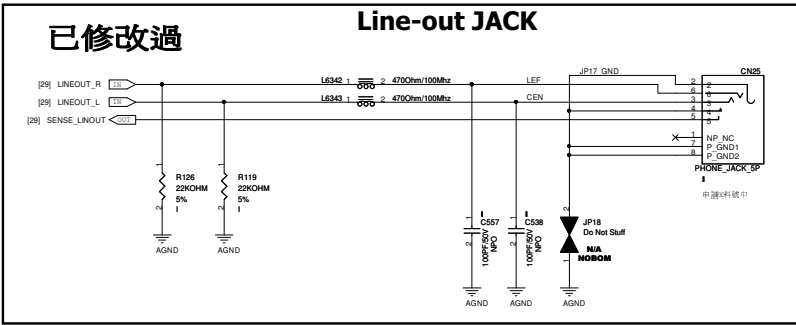
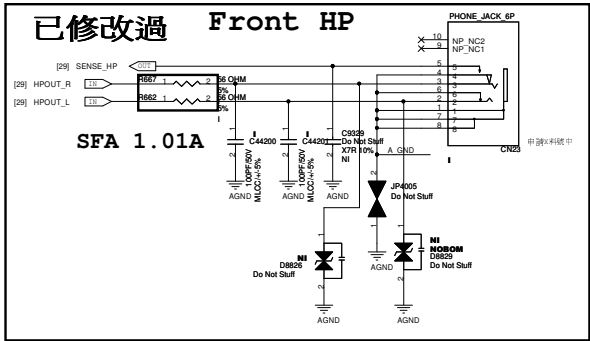
SFA 1.01A

SFA 1.01A

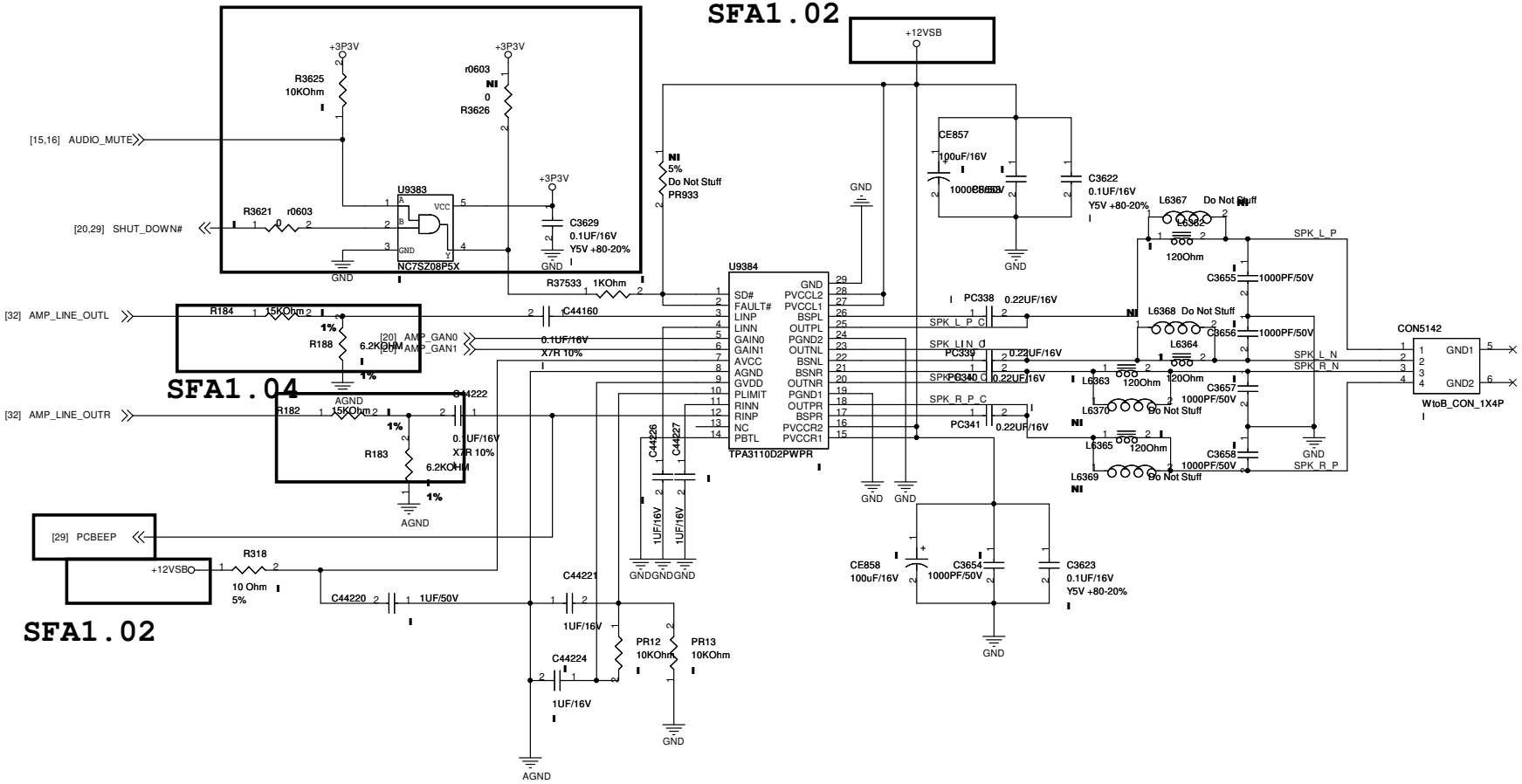
From SB

PEGATRON Title : Codec ALC269Q			
PEGATRON CORPORATION		Engineer: Jerry, Hsuan	
Size A3	Project Name IPPSB-FA	Rev 1.01	
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PLACE NEAR front audio CODEC FOR EMI

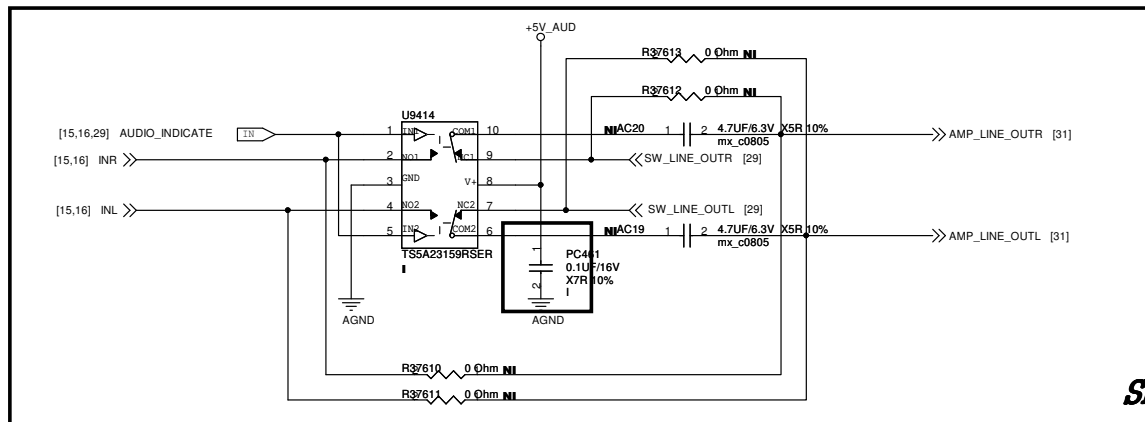


SFA1.02



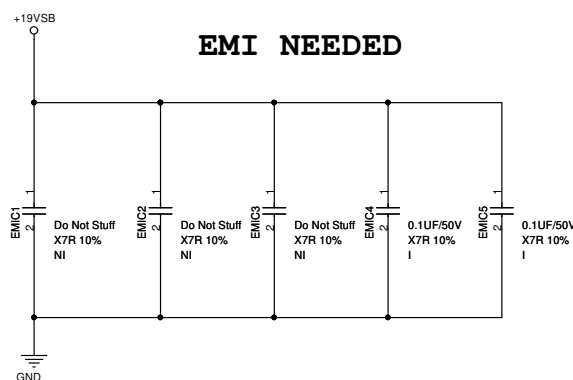
SFA1.02

PEGATRON Title : Amp TPA3100D2			
PEGATRON CORPORATION		Engineer: Jerry, Hsuan	
Size	Project Name		Rev
A3	IPPSB-FA		1.01
Date: Wednesday, April 27, 2011		Sheet	31 of 79

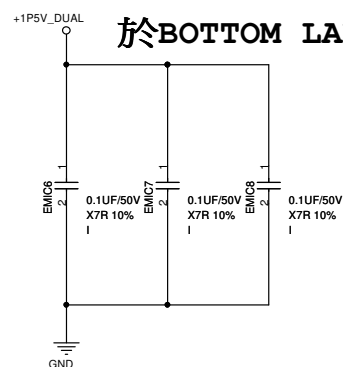


SFA1.04

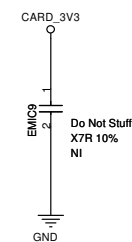
### EMI NEEDED



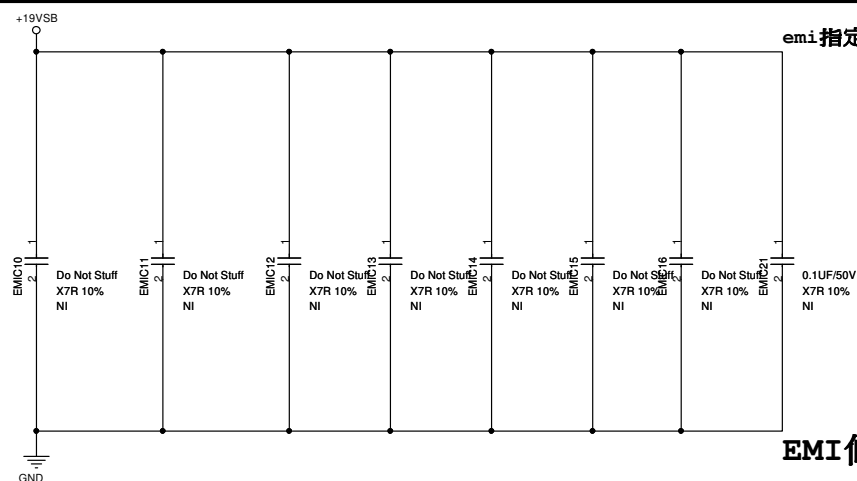
### 於BOTTOM LAYER 上



### 於TOP LAYER 上

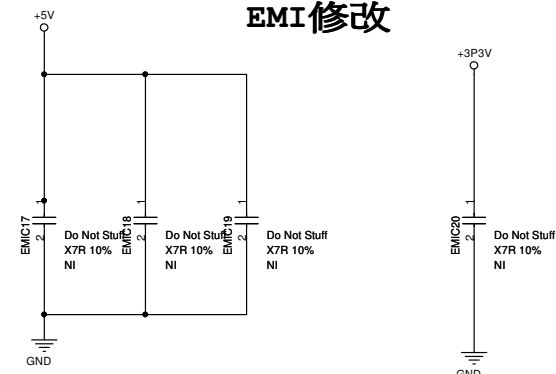


### emi指定位置



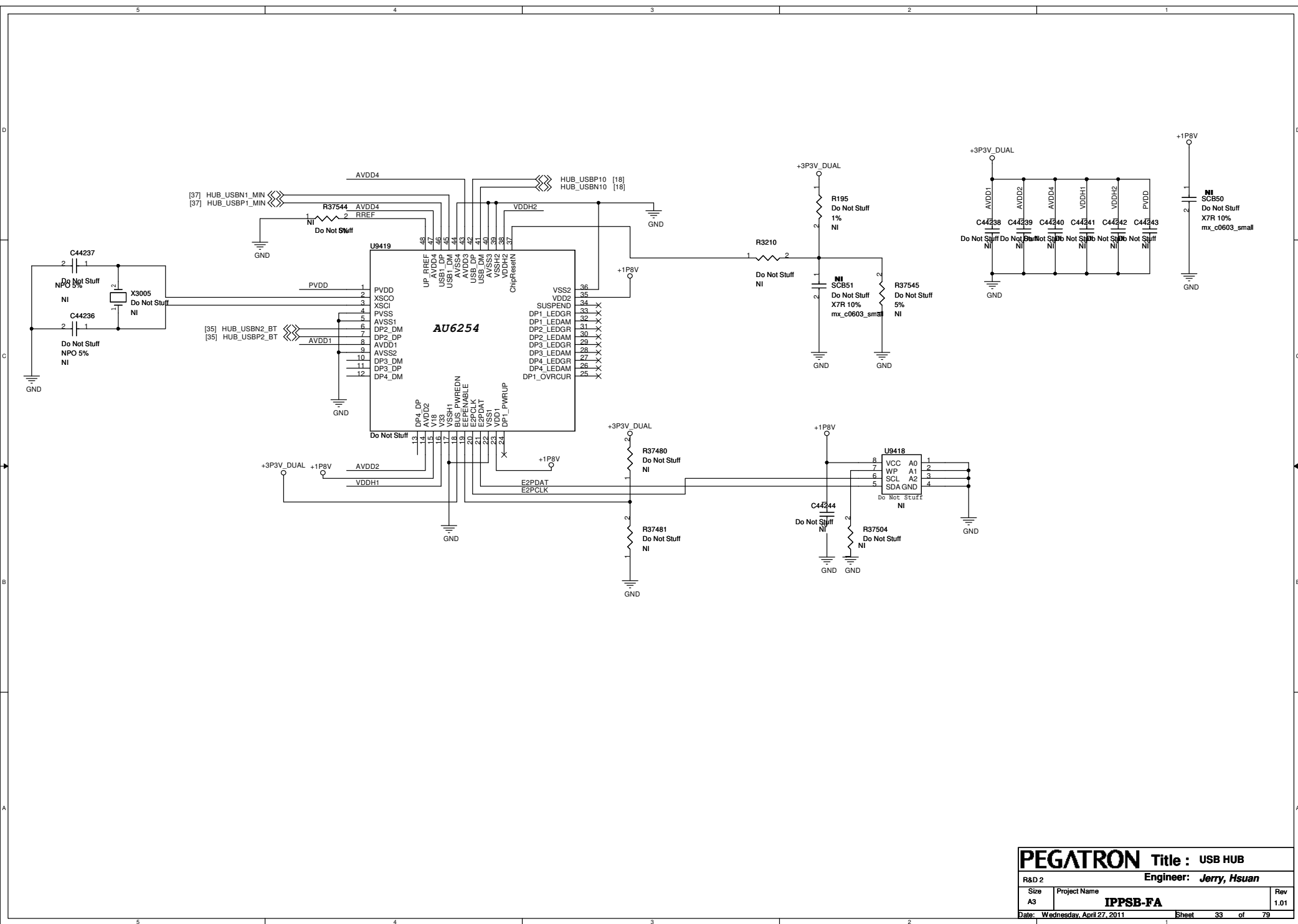
### EMI修改

### EMI修改



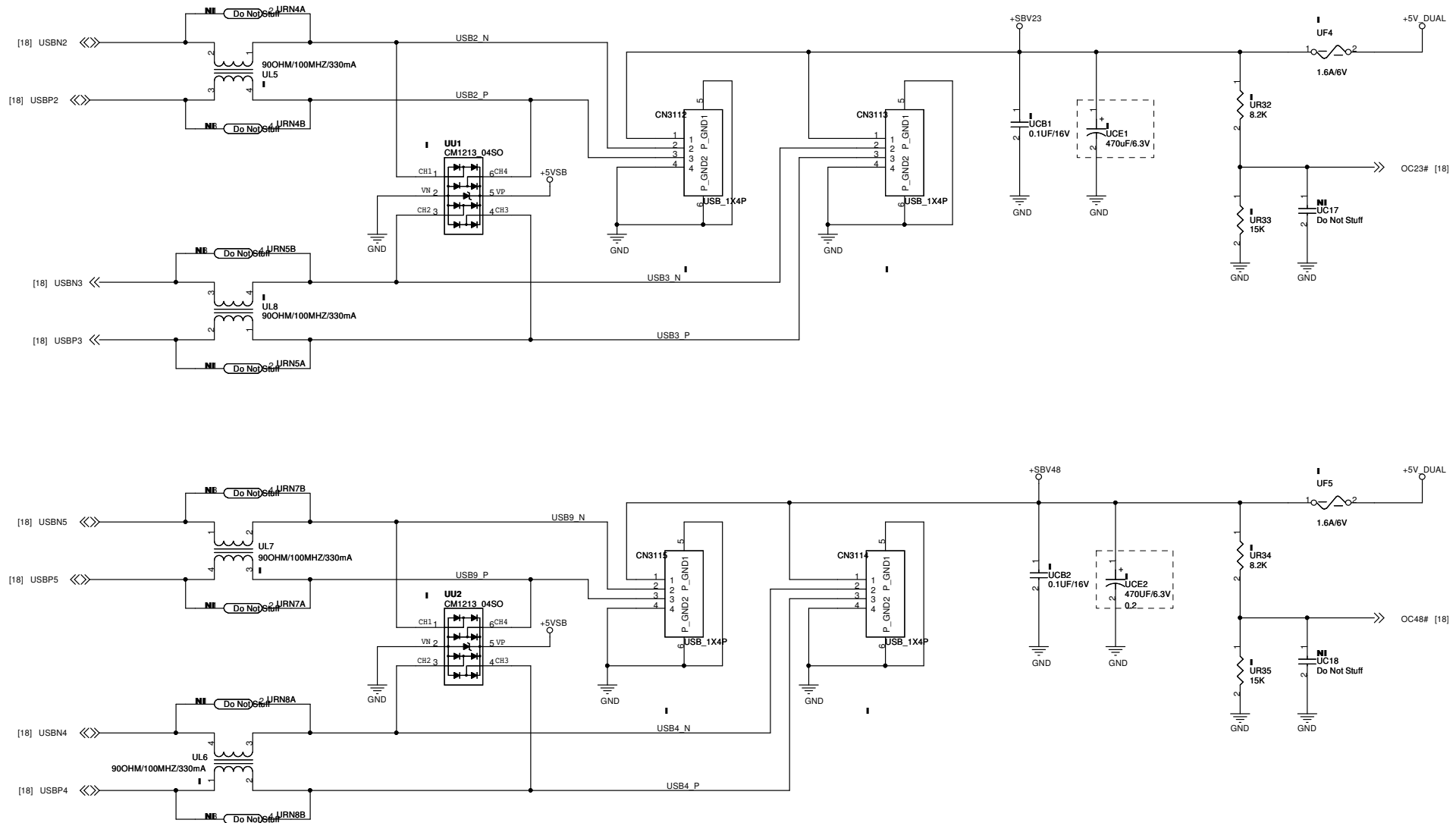
PEGATRON		Title : Amp SW & EMI	
PEGATRON CORPORATION		Engineer: Jerry, Hsuan	
Size A3	Project Name IPPSB-FA	Date: Wednesday, April 27, 2011	Rev 1.01
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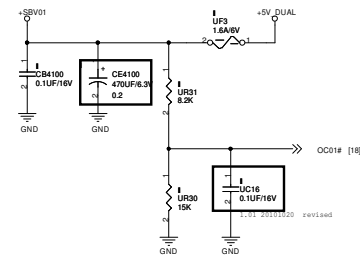
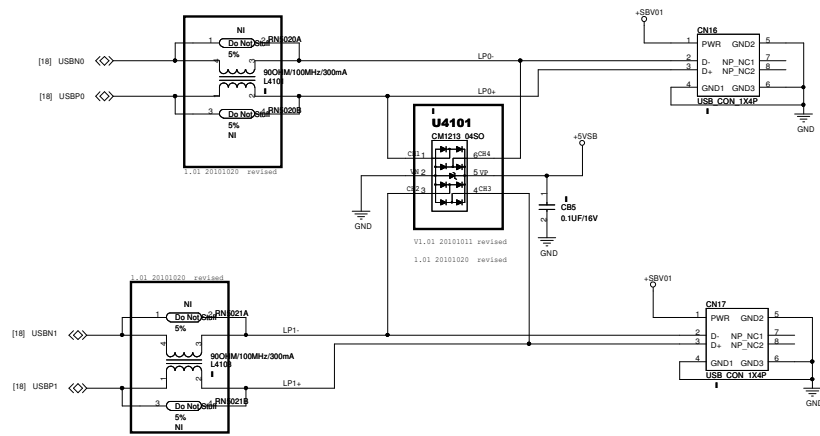
整頁修改過

# Rear USB2.0 \*4



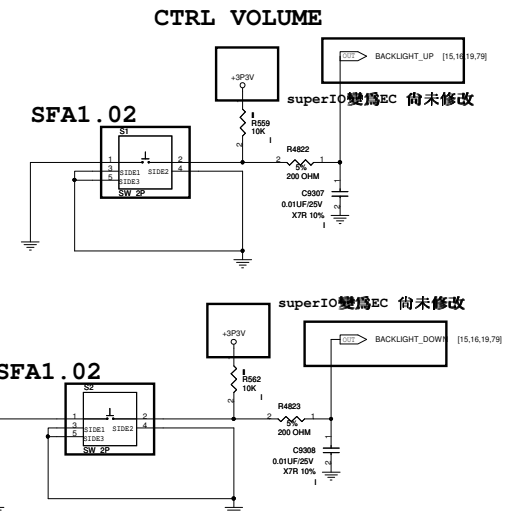
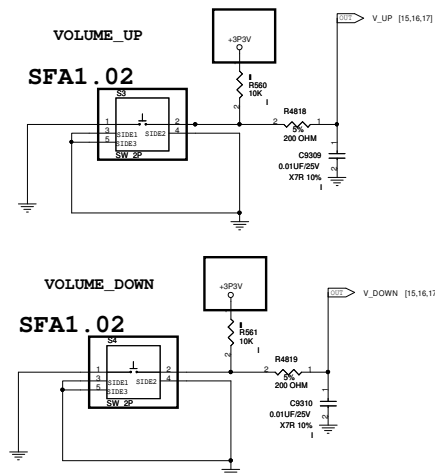
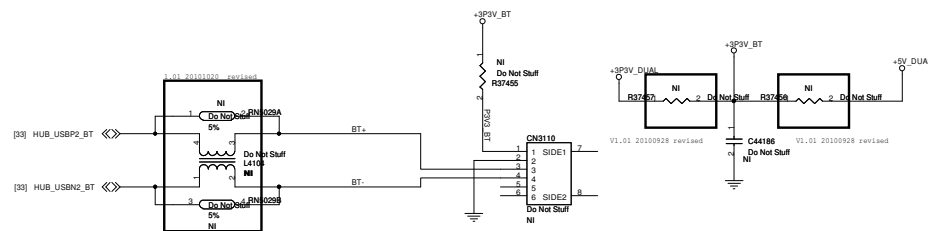
<b>PEGATRON</b>		<b>Title : Rear USB</b>	
PEGATRON CORPORATION		<b>Engineer: Mike Yen</b>	
Size A3	Project Name <b>IPPSB-FA</b>		Rev 1.01
Date: Wednesday, April 27, 2011		Sheet	34 of 79

已修改過

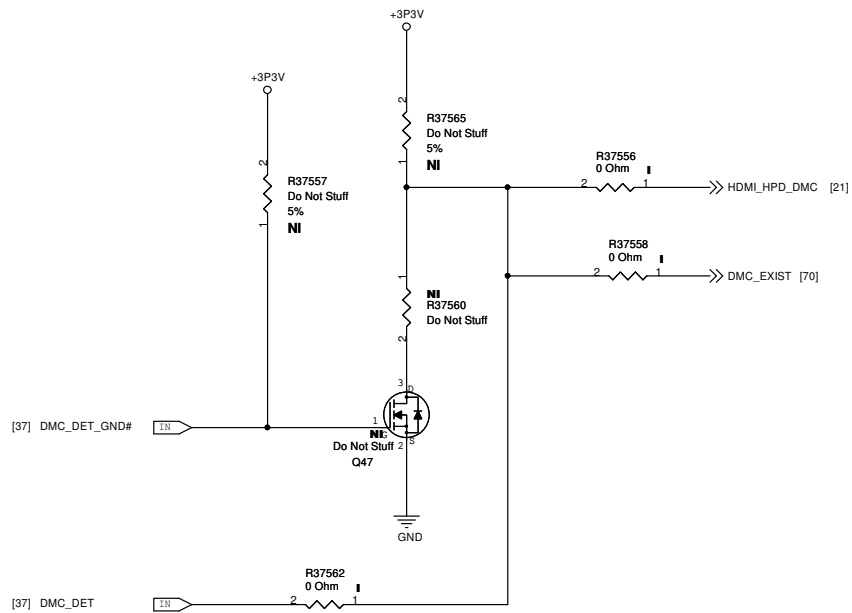
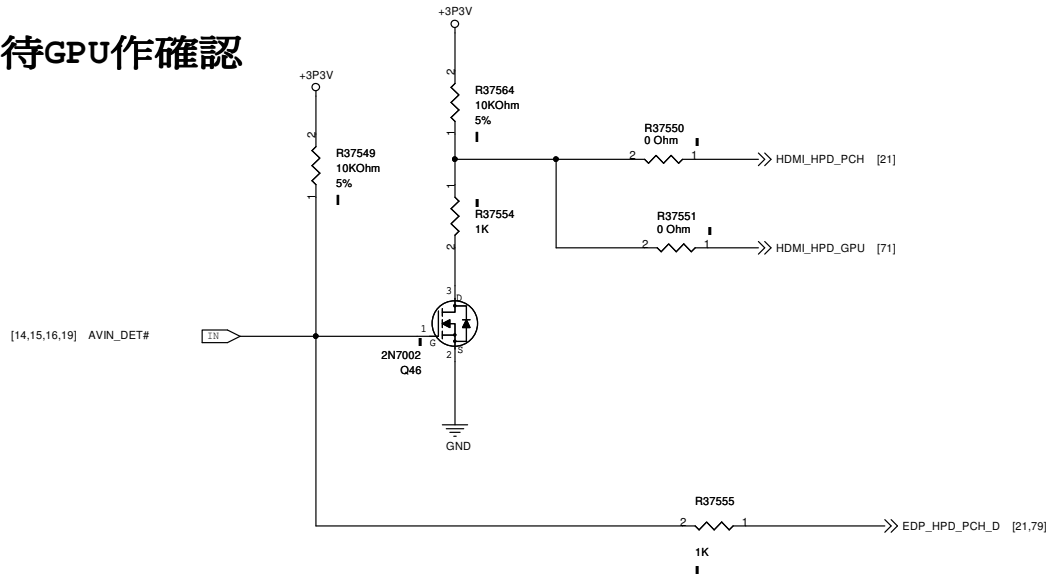


另外增加  
Internal I/O  
BLUE TOOTH

the DMC device connected BT symbols is needed

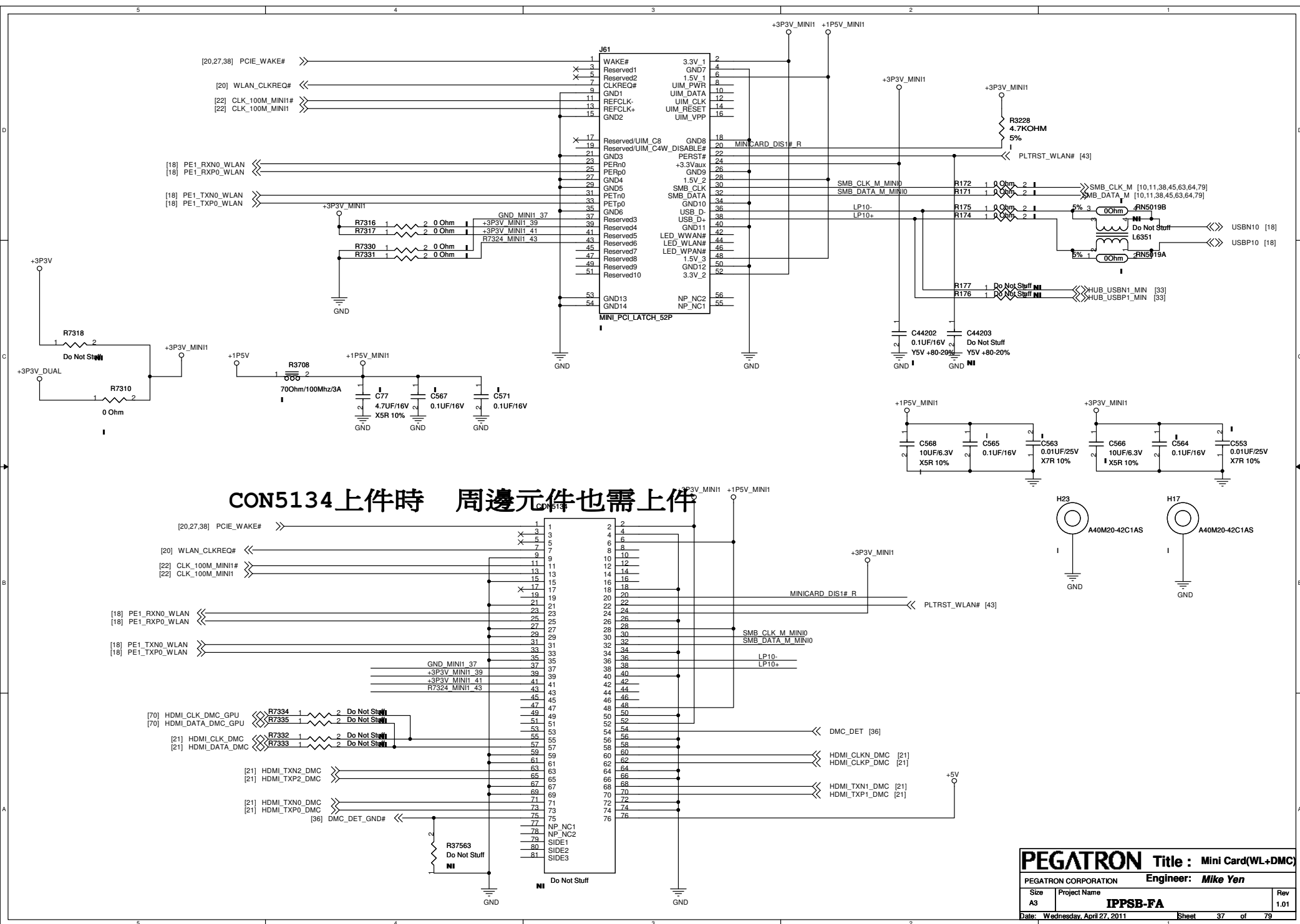


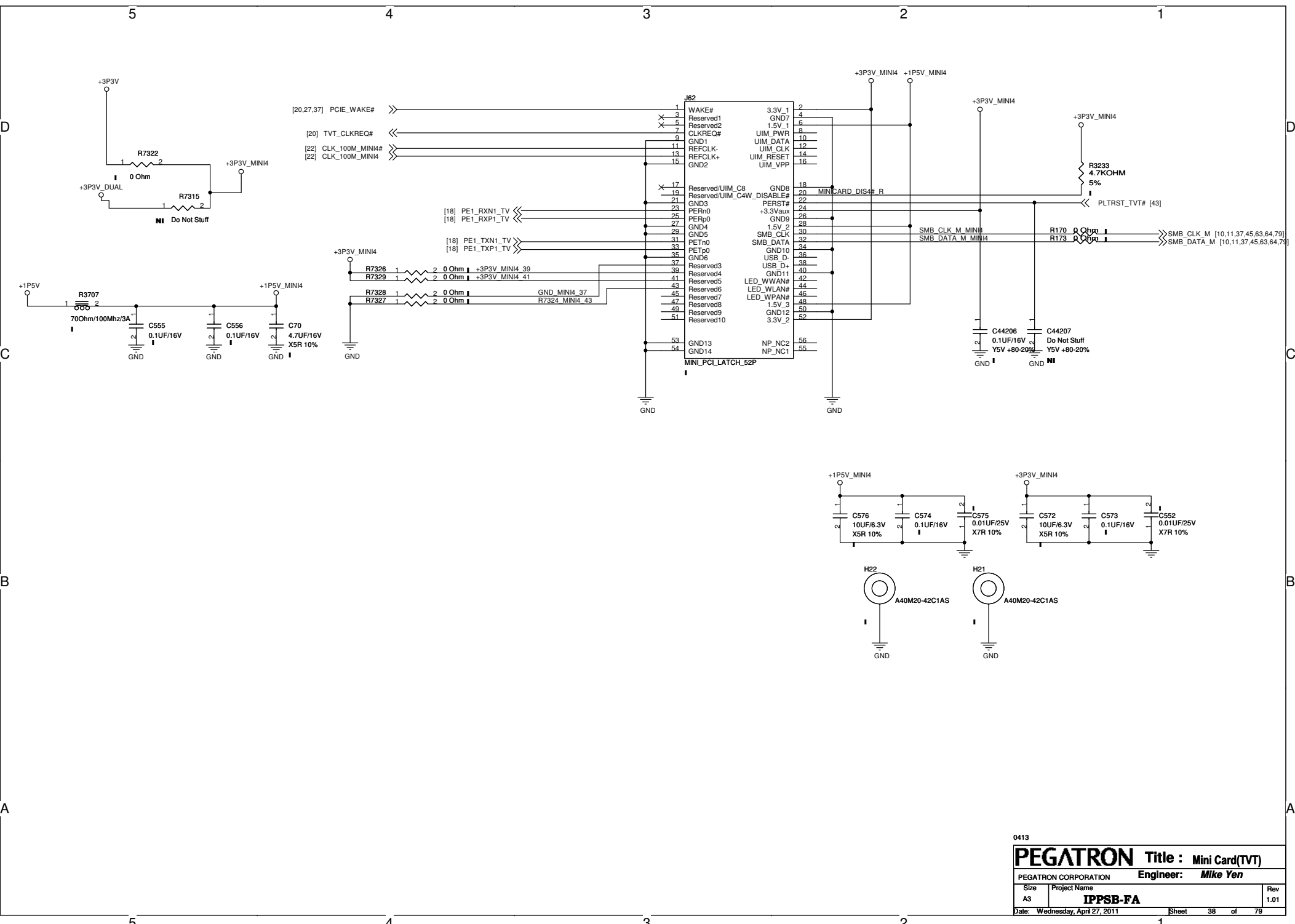
待GPU作確認



0413

<b>PEGATRON</b>		<b>Title :</b> HPD DET	
<b>R&amp;D 2</b>		<b>Engineer:</b> <i>Jerry, Hsuan</i>	
<b>Size</b> A3	<b>Project Name</b> <b>IPPSB-FA</b>	<b>Rev</b> 1.01	
<b>Date:</b> Wednesday, April 27, 2011		<b>Sheet</b>	36 of 79





0413

**PEGATRON** Title : Mini Card(TVT)

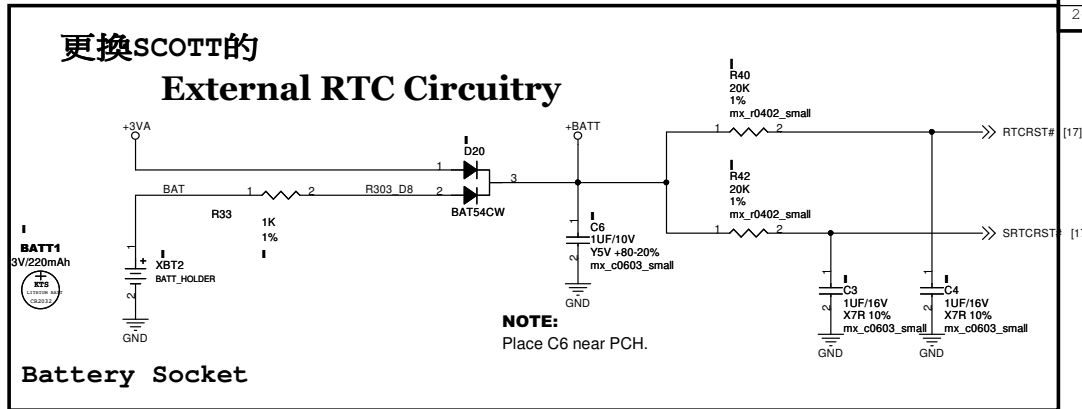
PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPSPB-FA Rev 1.01

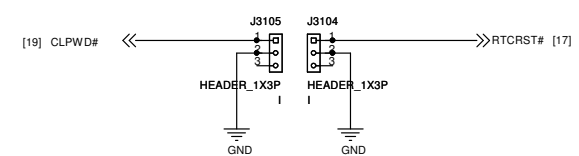
Date: Wednesday, April 27, 2011 Sheet 38 of 79

## CLR CMOS CIRCUIT

## CLR PASSWORD CIRCUIT



PASSWORD
1-2 CLEAR
2-3 Default

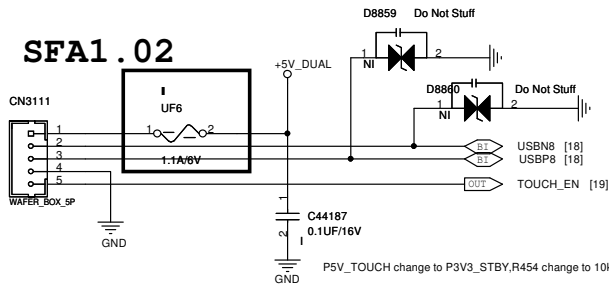


CMOS RTC
1-2 CLEAR
2-3 Default

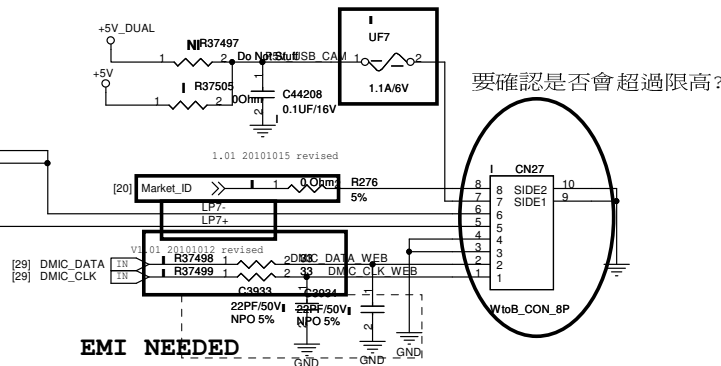


## TOUCH

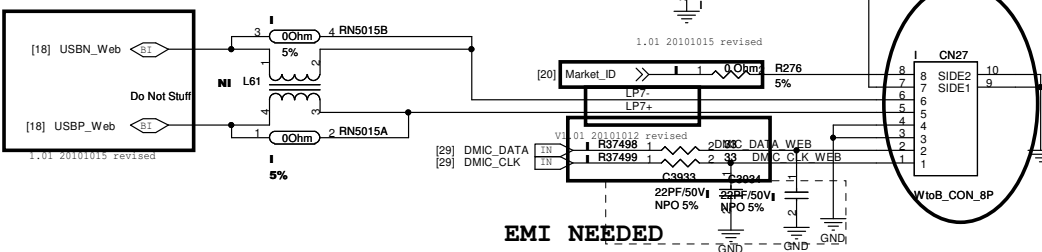
### SFA1.02

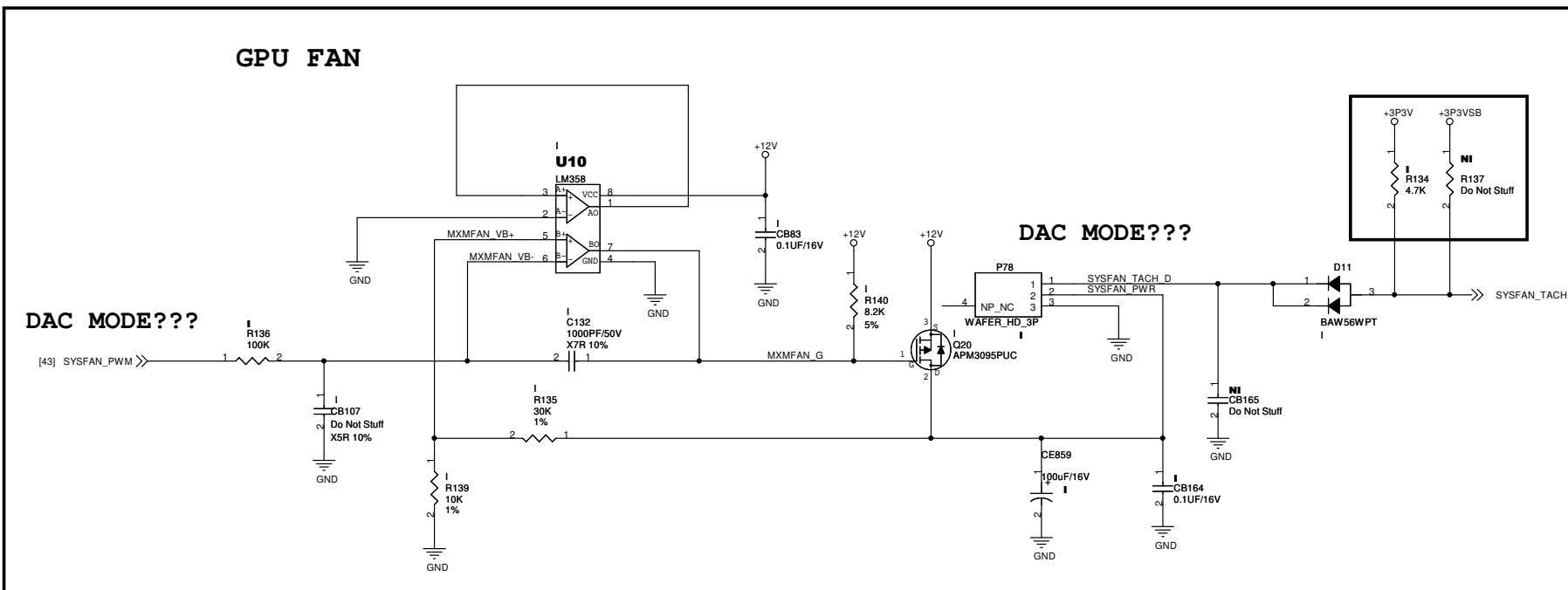
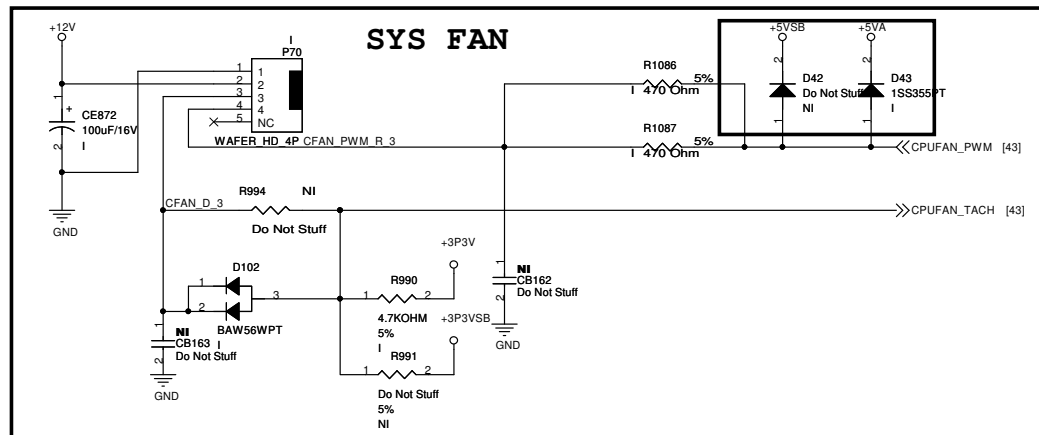


### SFA1.03

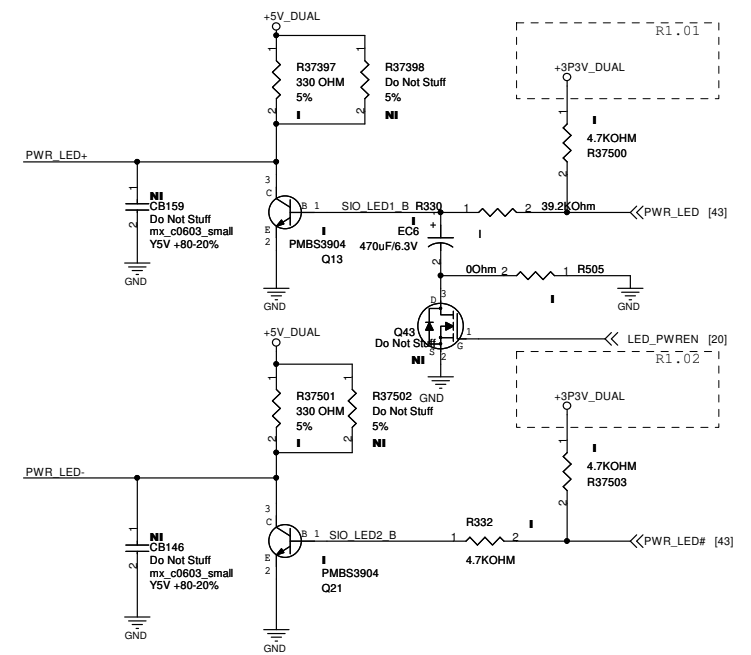
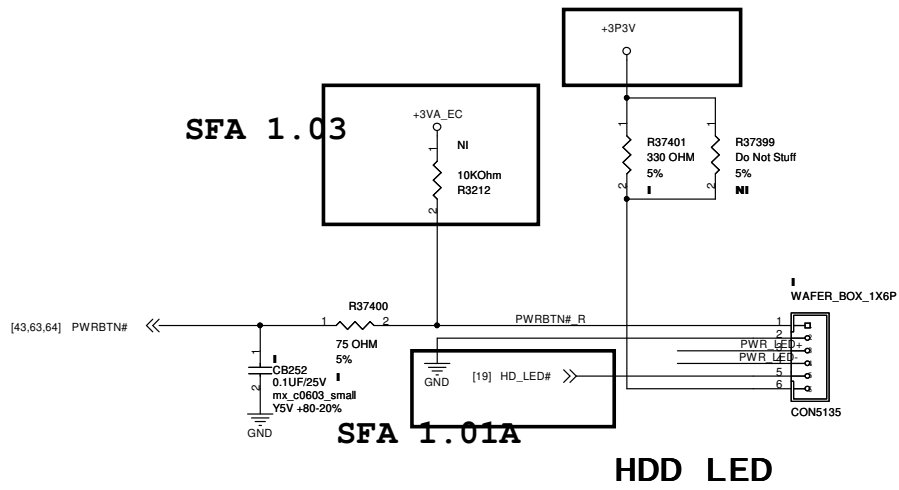


## 已修改過 CAMERA MODULE

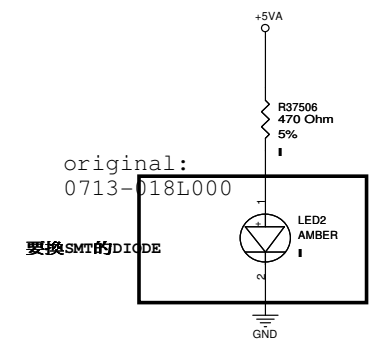








## Power supply LED

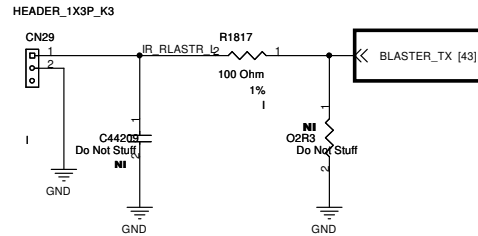


original:  
0713-018L000

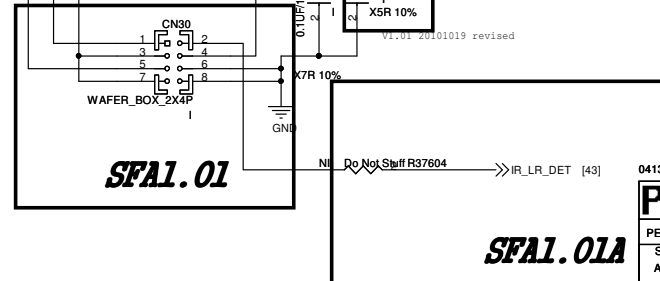
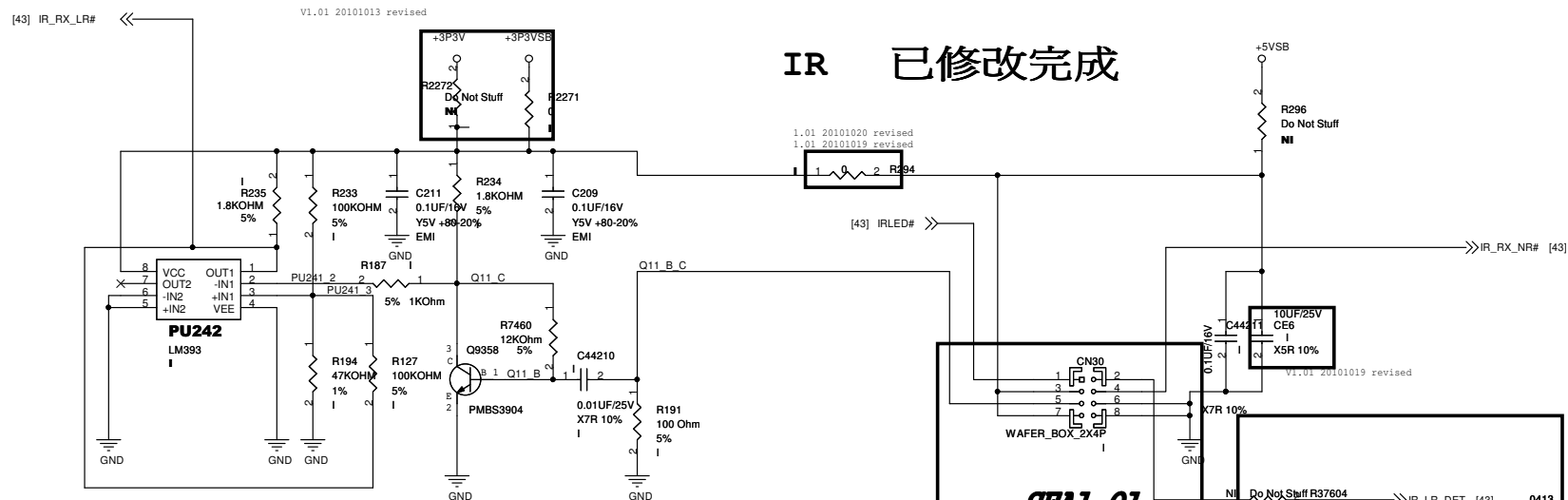
要換SMT的DIODE

0413		PEGATRON Title : PWE LED	
PEGATRON CORP.		Engineer: Mike Yen	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Wednesday, April 27, 2011		Sheet	41 of 79

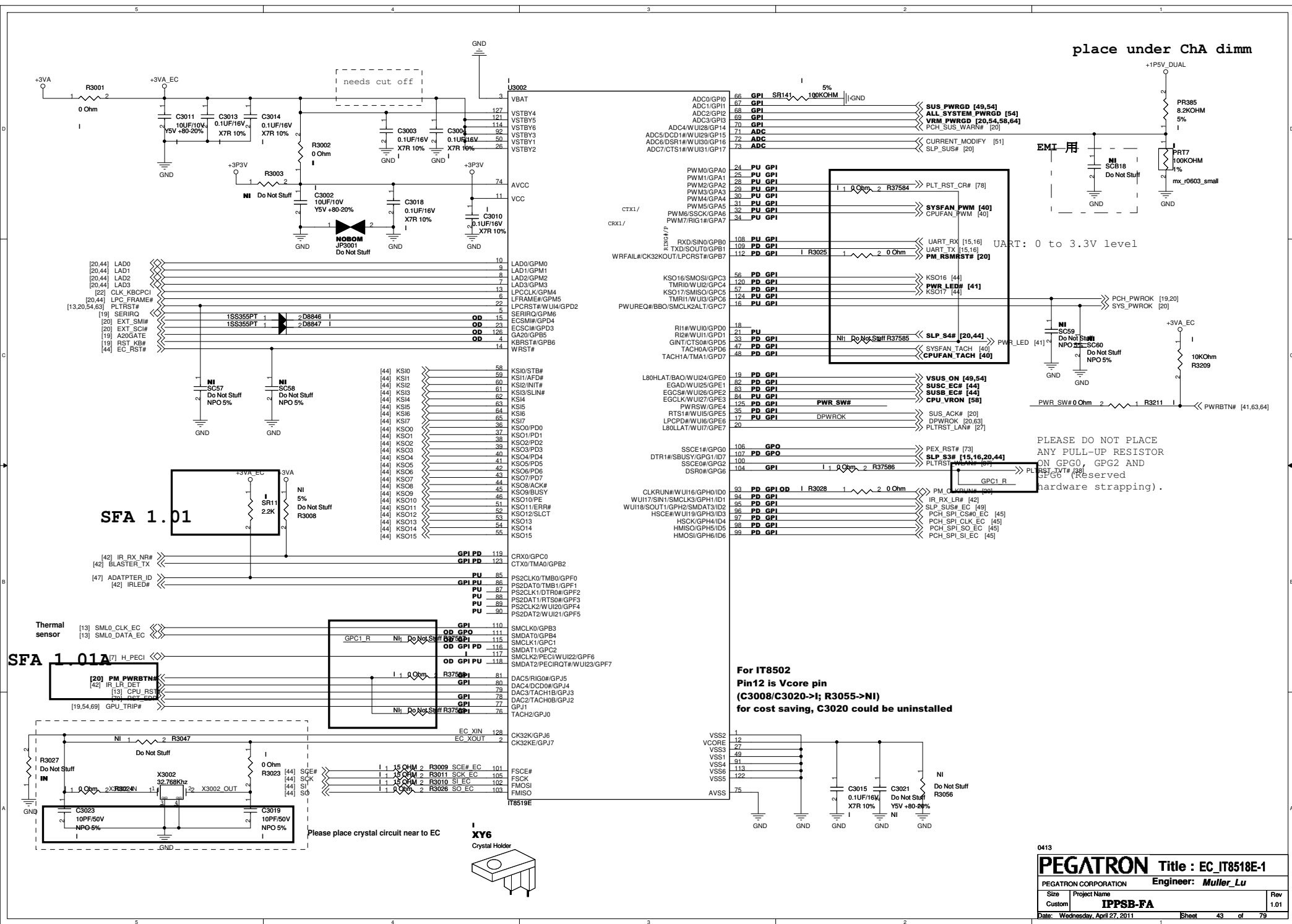
# 線條未改 IR Blaster



# IR 已修改完成



<b>PEGATRON</b>		Title : IR LEDs	
PEGATRON CORPORATION		Engineer: <i>Mike Yen</i>	
Size A3	Project Name <b>IPPSB-FA</b>		Rev 1.01
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[illegible]

### For Instant Key & Switch

For EC PU/PD


Timing diagram for J3103 VP showing signals KS00 through KS17. The diagram includes a vertical axis for time (0 to 28 ns) and a horizontal axis for signals. KS00-KS17 are shown as digital signals. A dashed box highlights a specific signal transition. A legend at the bottom identifies the signals: KS00, KS01, KS02, KS03, KS04, KS05, KS06, KS07, KS08, KS09, KS010, KS011, KS012, KS013, KS014, KS015, KS016, KS017, KS10, KS11, KS12, KS13, KS14, KS15, KS16, KS17. A note indicates that the signals are not shown for the first 12 ns of the test.

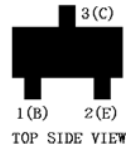
The diagram shows the electrical connection for the EC\_RST# signal. It starts with a pin labeled [49\_54] FORCE\_OFF#. This pin is connected to a 100KOHM resistor (R3118). The other end of R3118 is connected to the cathode of a 1SS355PT diode (D3108). The anode of D3108 is connected to a 100KOHM resistor (R3117). The other end of R3117 is connected to the cathode of another 1SS355PT diode (D3107). The anode of D3107 is connected to a 4.7UF/10V capacitor (C3103), which is then connected to ground. The signal line after D3107 is labeled EC\_RST# [43] and 'To EC RESET'.

[illegible]

The schematic diagram illustrates the power management section of the PWR0K R Q. It features a +3P3V input connected to a network of resistors and MOSFETs. A P-channel MOSFET (Q7) is used for the main power switch, with its gate controlled by a voltage divider consisting of R55 and R56. An N-channel MOSFET (Q14) is used for a secondary switch or regulation, with its gate controlled by a divider of R15 and R56. The output of the circuit is labeled PWR0K R Q.

[17,27] SMB\_DATA <<>>

[17,27] SMB\_CLK 



**SPI BIOS ROM - 04 Mb or 32Mb**

**E16:** Dual SPI BIOS ROM  
F3R1 and F3R7 are 33ohm.

**F3U2:** 64Mb: 05X00Z2GE330  
Dual SPI BIOS ROM  
F3R5 and F3R6, F3R8 and F3R9 are 33ohm.

**NOTE:** Dual SPI BIOS ROM  
F3R1 and F3R7 are 33ohm.

**NOTE:** Dual SPI BIOS ROM  
F3R5 and F3R6, F3R8 and F3R9 are 33ohm.

**E16:12**  
MINI\_JUMPER

**BOTTOM SIDE VIEW**  
**TOP SIDE VIEW**

**NOTE:**  
Dual SPI BIOS ROM  
F3R1 and F3R7 are 33ohm.

64Mb: 05X00Z2GE330

**NOTE:**  
Dual SPI BIOS ROM  
F3R5 and F3R6, F3R8 and F3R9 are 33ohm.

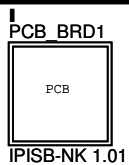
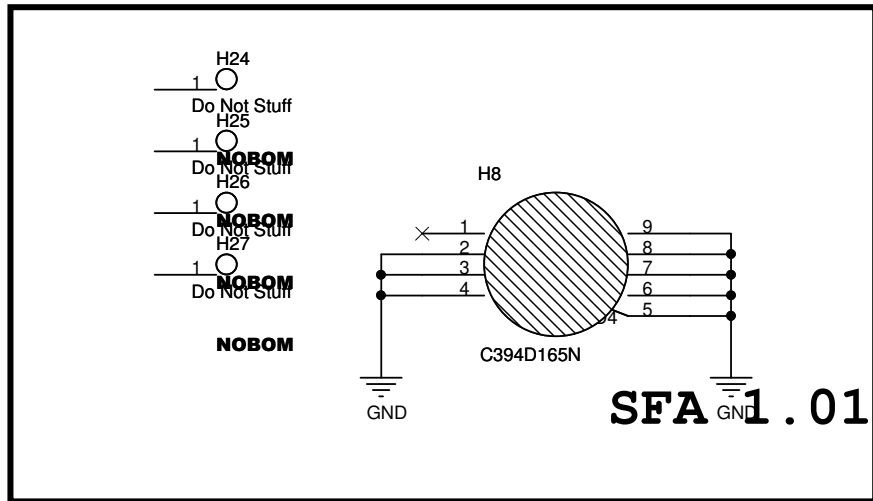
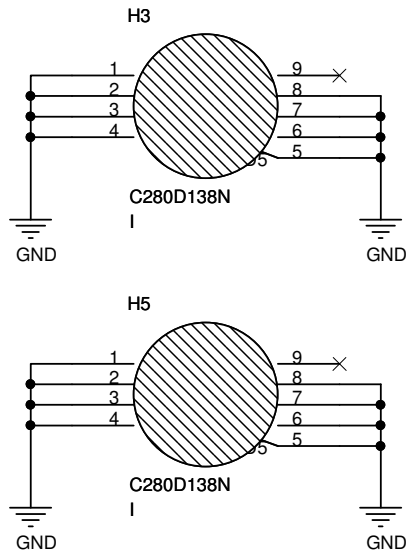
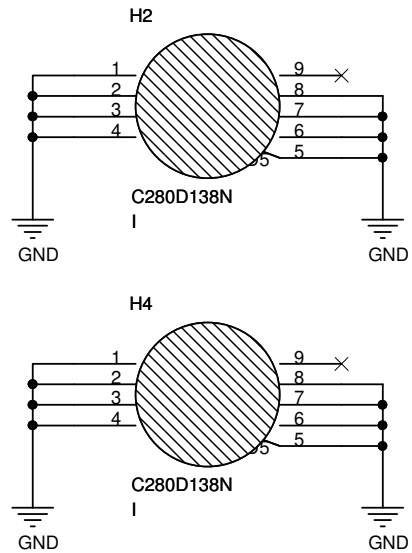
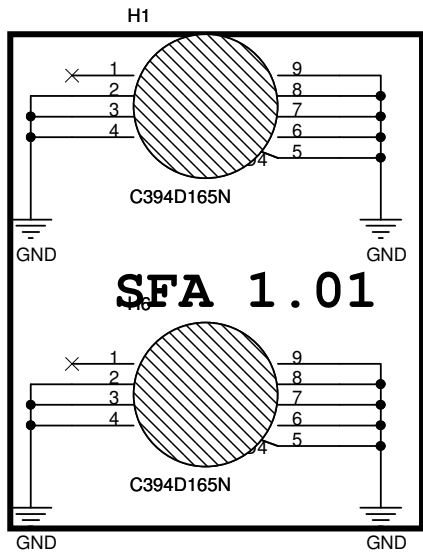
**PEGATRON DT-MB RESTRICTED SECRET**

**PEGATRON** Title : SM BUS & SPI ROM

PEGATRON CORPORATION	Engineer:	XXXX-XX
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Size	Project Name	Rev
15	IBPSR-FA	

A3	IFFSB-FA	1.01
Date: Wednesday, April 27, 2011		Sheet 45 of 79



IPISB-NK 1.01

VESA mount hole

0413

<b>PEGATRON</b>		Title : SCREW HOLE	
PEGATRON CORPORATION		Engineer: <b>Mike Yen</b>	
Size A	Project Name <b>IPPSB-FA</b>		Rev 1.01
Date: Wednesday, April 27, 2011		Sheet	46 of 79

[illegible]

PAGATRON DT-MB RESTRICTED SECRET			
<b>PAGATRON</b>		Title : UVP, OVP & +19VSB	
PAGATRON CORPORATION		Engineer: Mike Yen	
Size A3	Project Name <b>IPPSB-FA</b>		Rev 1.01
Date: Wednesday, April 27, 2011		Sheet 47 of 79	



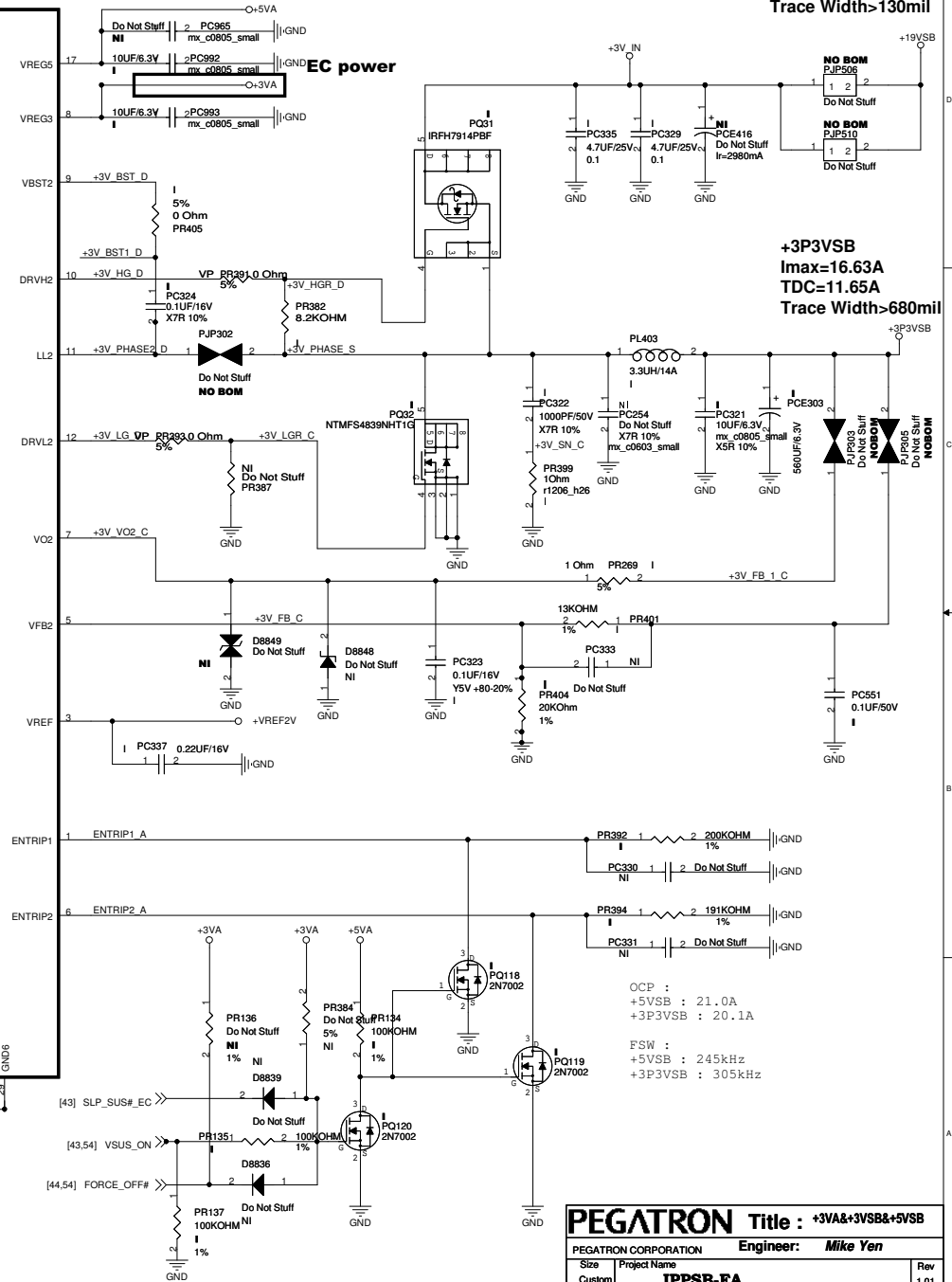
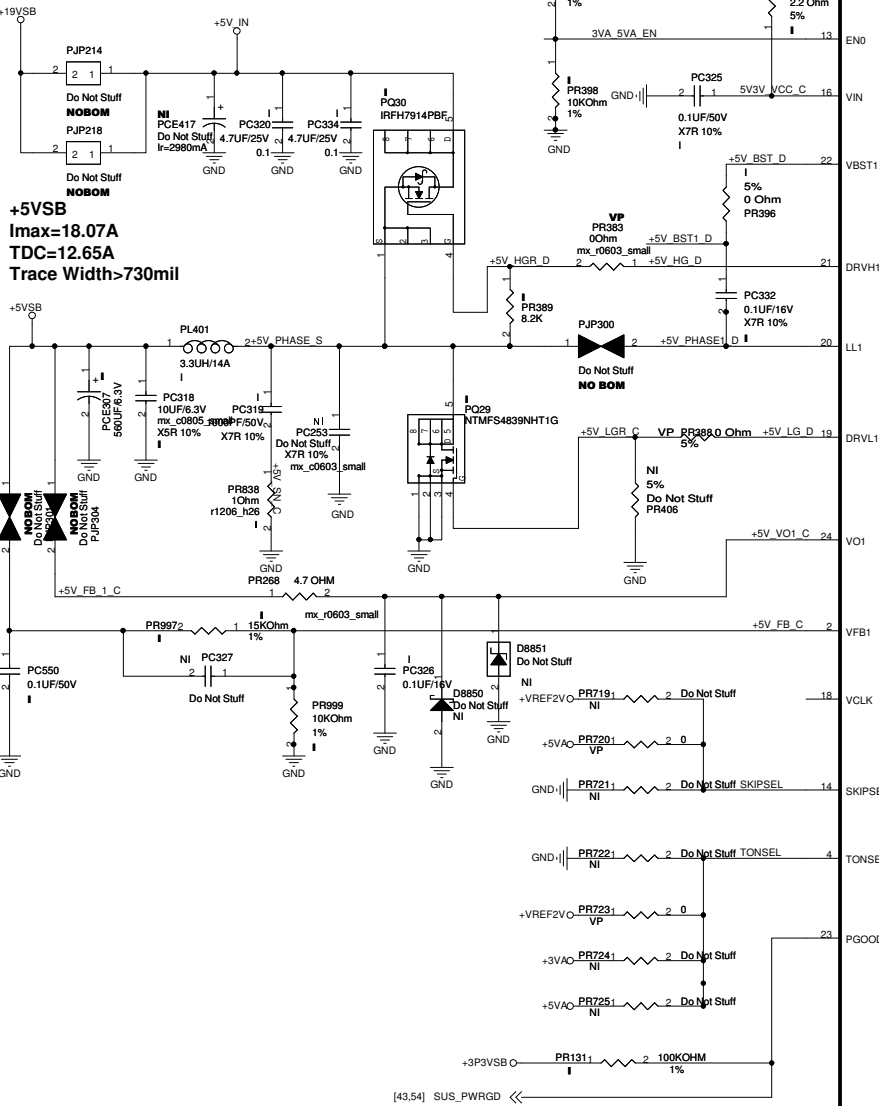


**+19VSB**  
**Iin=5.95A**  
**Trace Width>240mil**

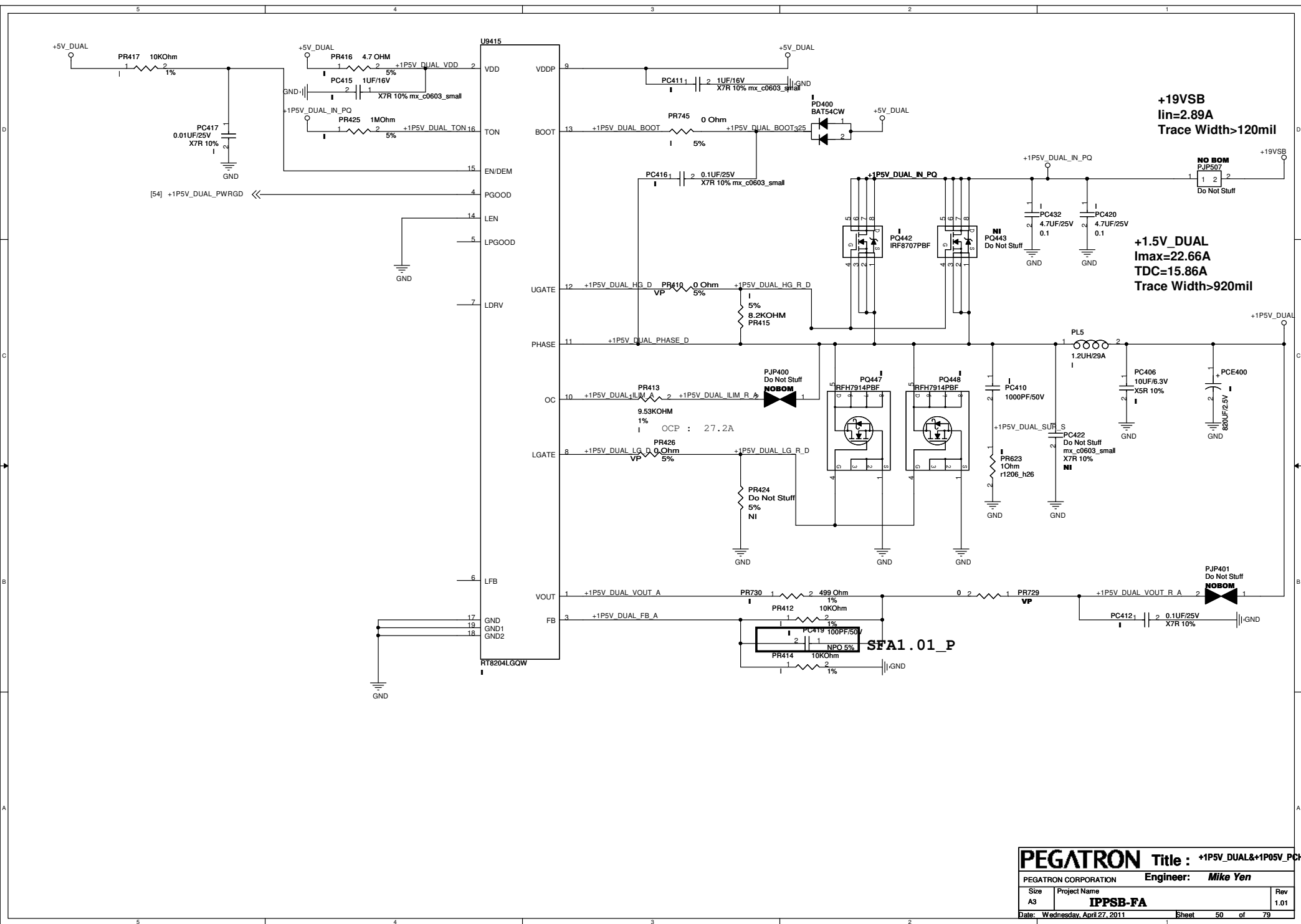
**+5VSB**  
**I<sub>max</sub>=18.07A**  
**TDC=12.65A**  
**Trace Width>730mil**

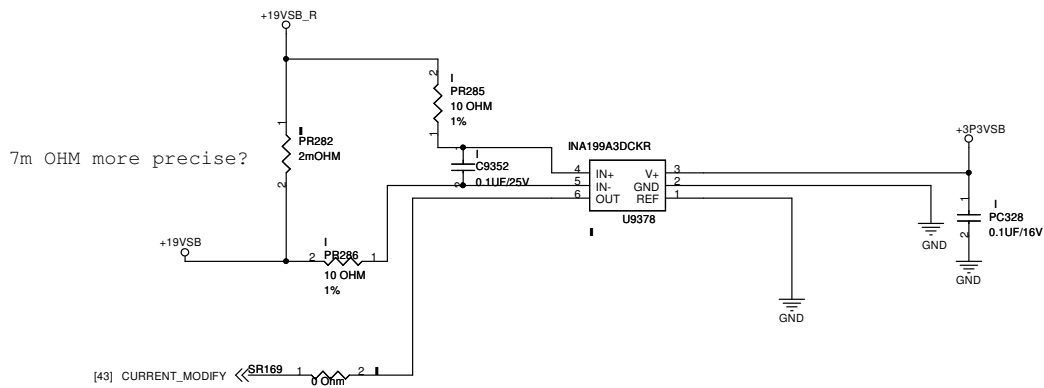
**+19VSB**  
**Iin=3.25A**  
**Trace Width>130mil**

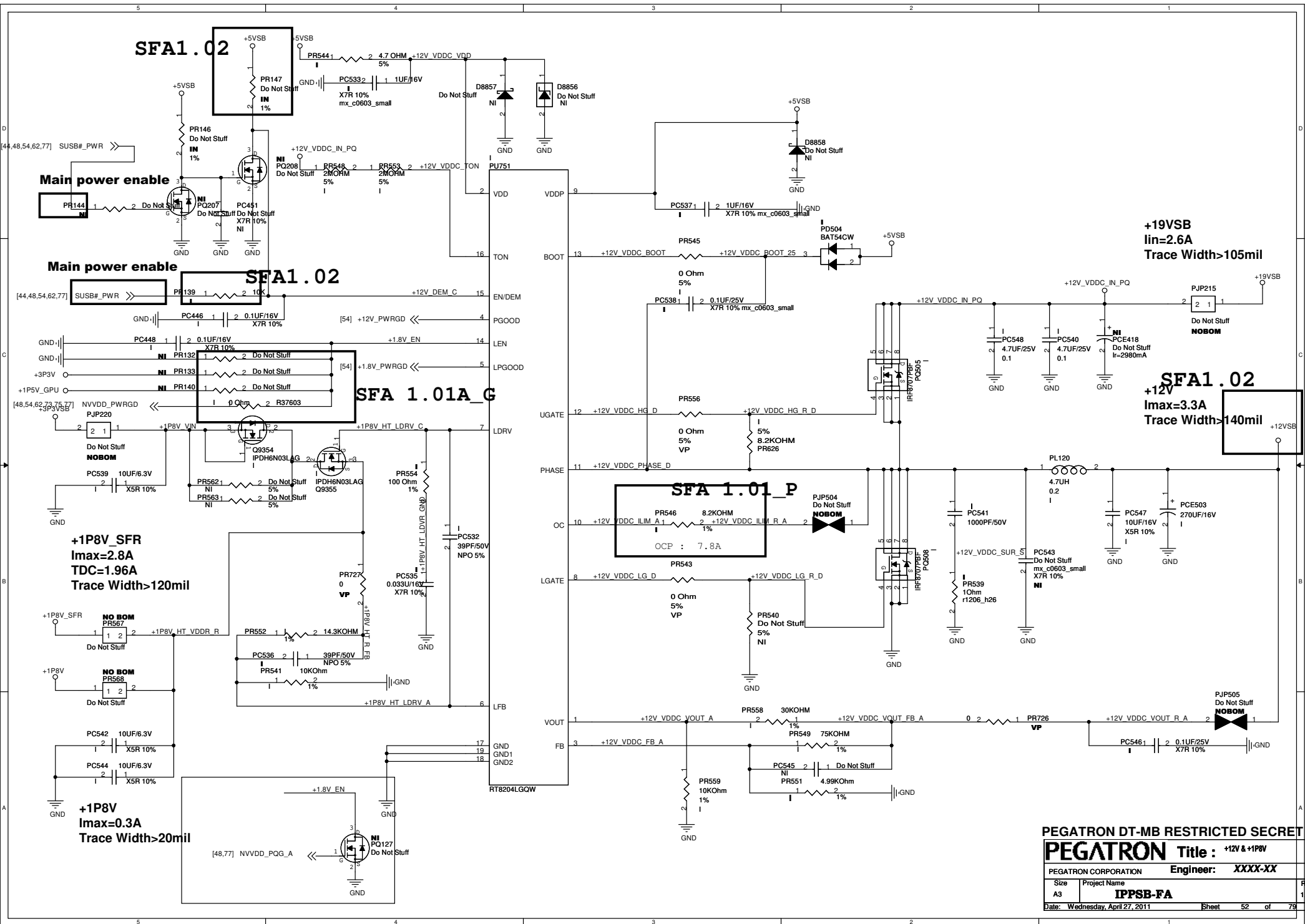
**+3P3VSB**  
**I<sub>max</sub>=16.63A**  
**TDC=11.65A**  
**Trace Width>680mil**

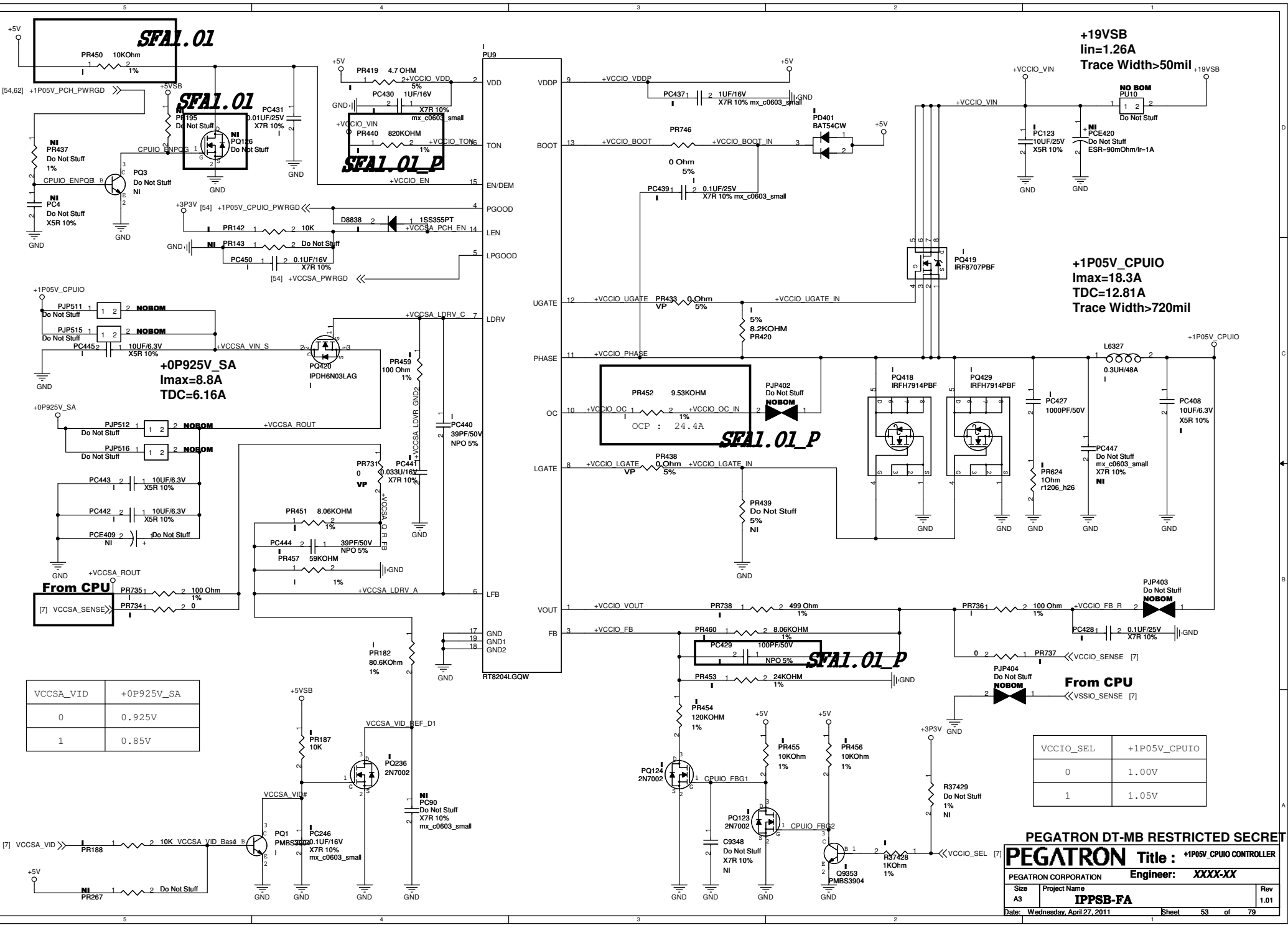


PEGATRON Title : +3VA&+3VSB&+5VSB			
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name		
Custom	IPPSB-FA		
Date: Wednesday, April 27, 2011	Sheet	49	of 79





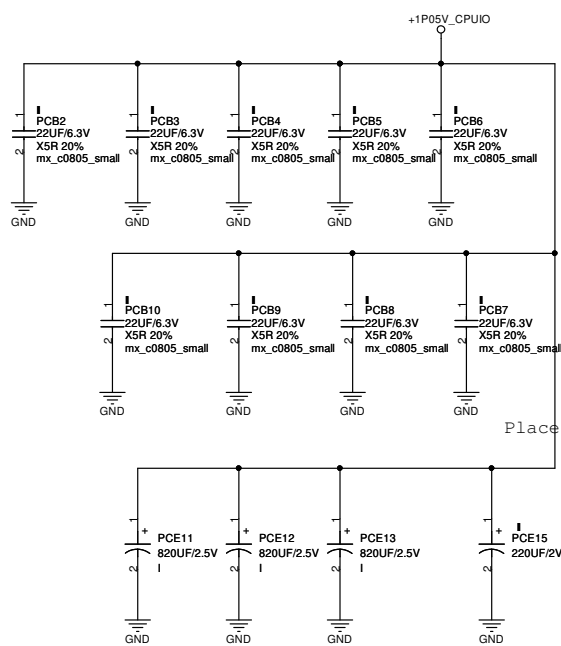
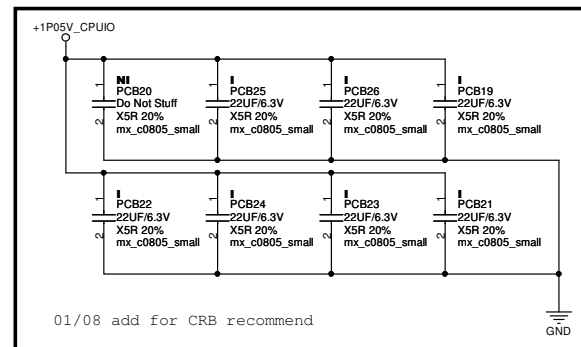
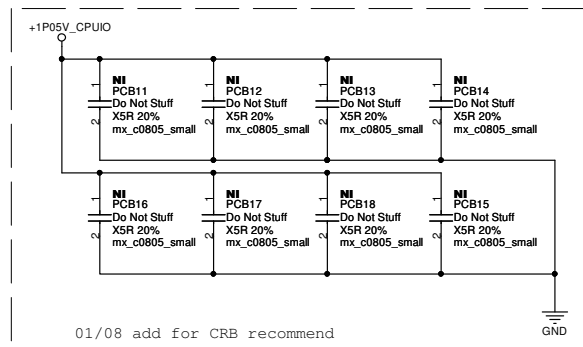




VCCSA_VID	+0P925V_SA
0	0.925V
1	0.85V

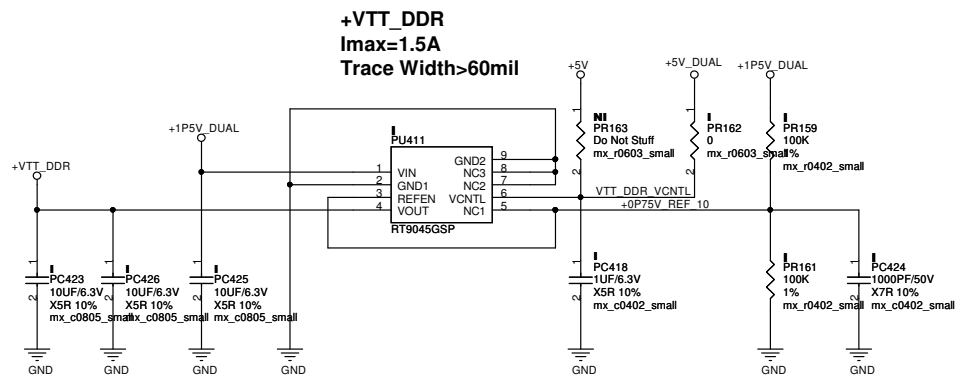
VCCIO_SEL	+1P05V_CPUIO
0	1.00V
1	1.05V





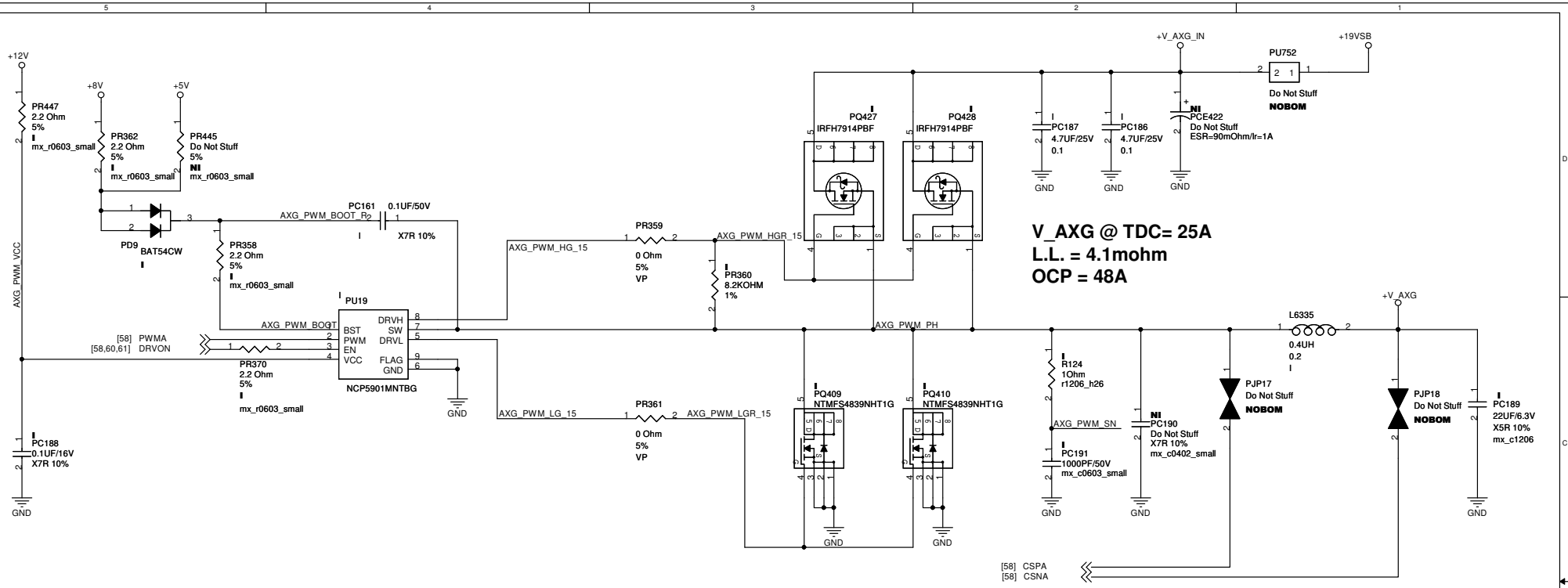
### VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560uF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22uF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2, 3
0805 placeholders	16				Backside	



PEGATRON Title : +VTT_DDR		
PEGATRON CORPORATION		Engineer: Mike Yen
Size A3	Project Name IPPSB-FA	Rev 1.01
Date: Tuesday, April 26, 2011	Sheet 56	of 79



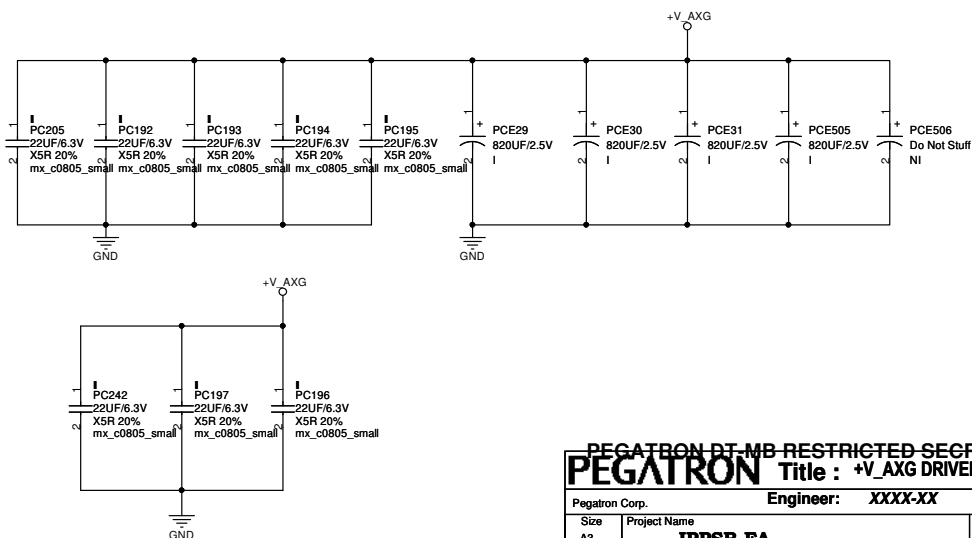


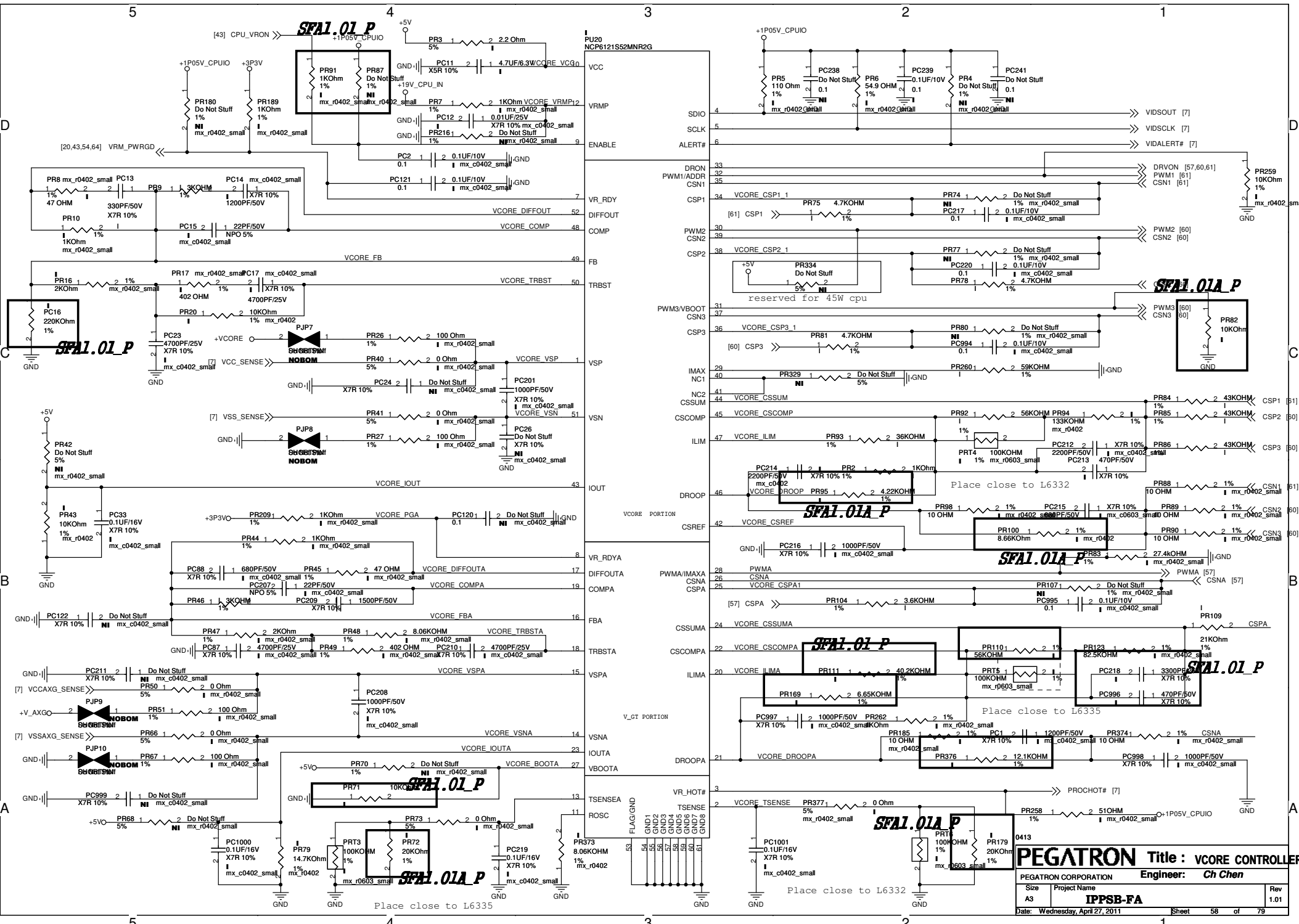
## Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2, 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1

PL-CAP \*4  
MLCC \*6



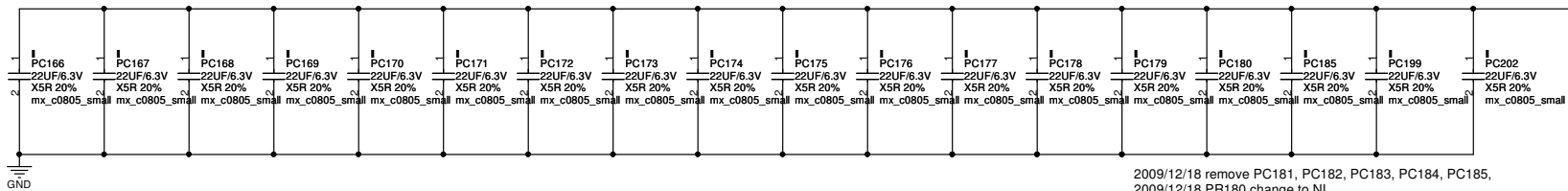
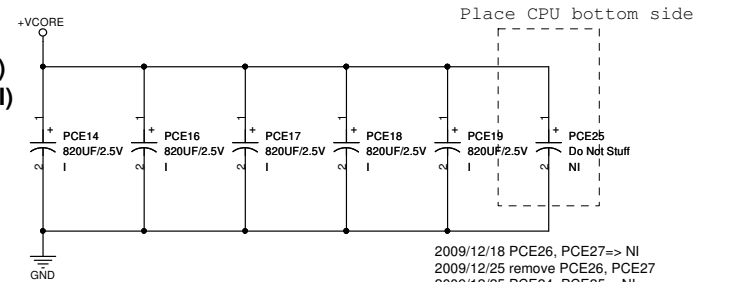


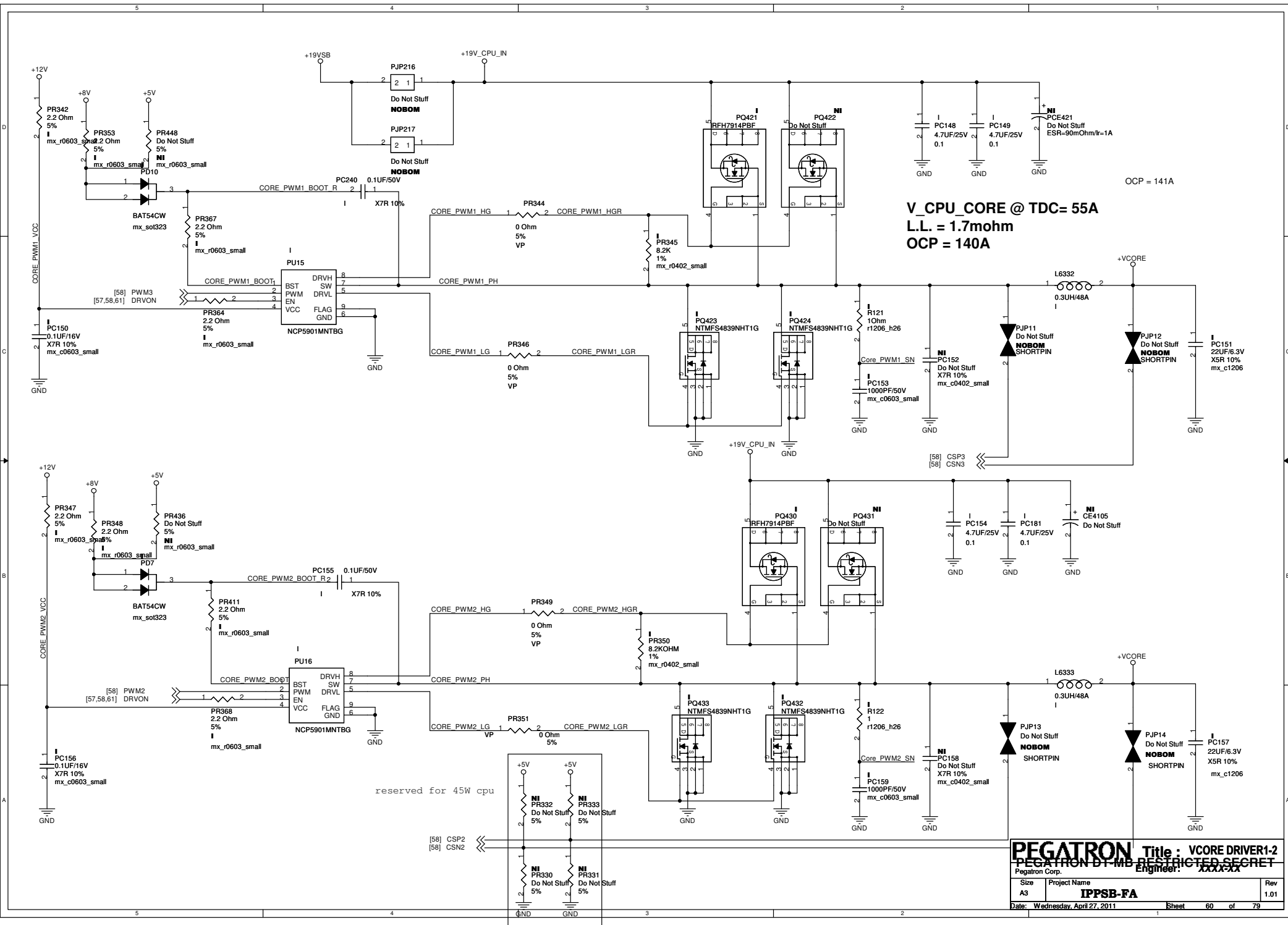
# Output CAP

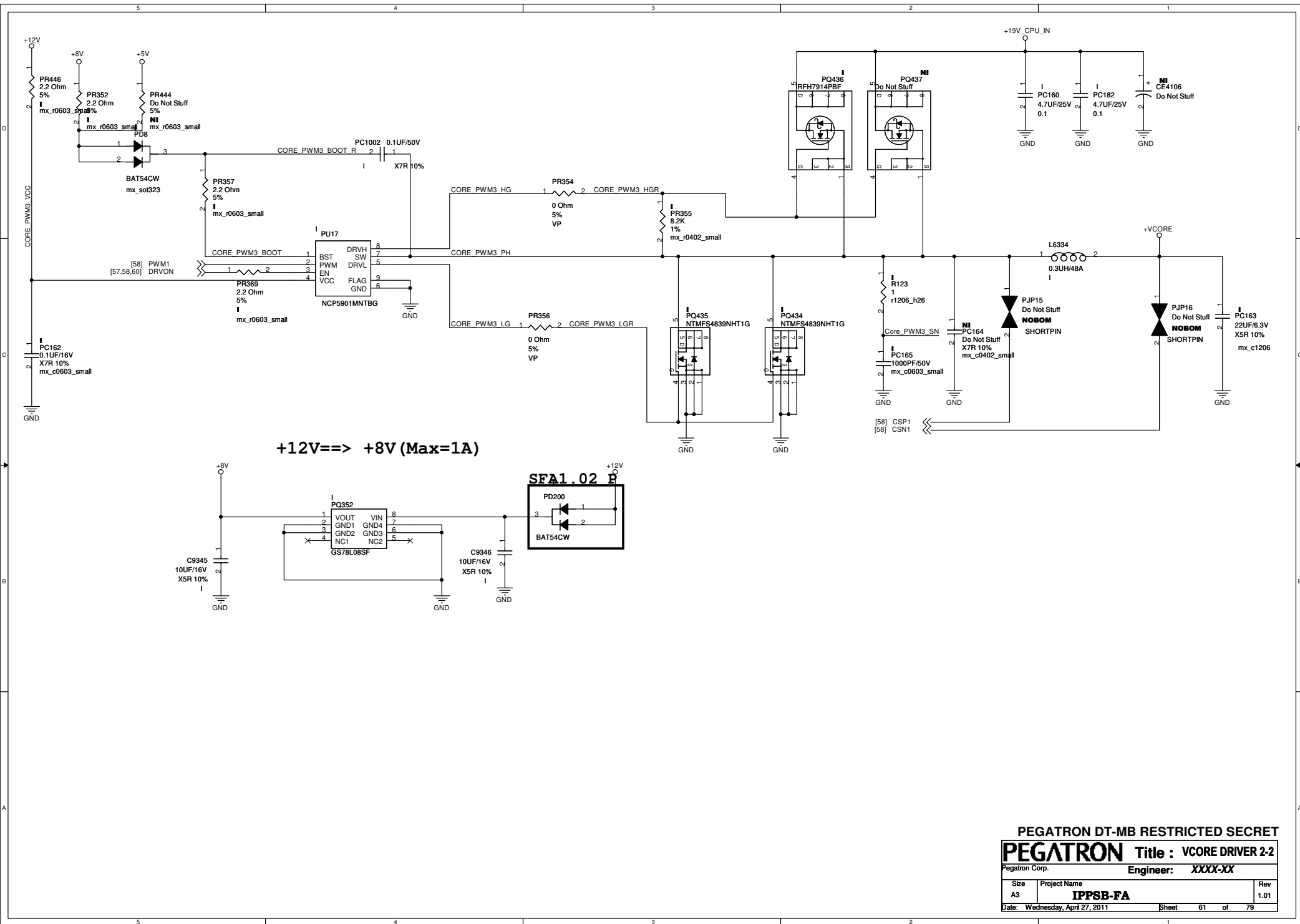
Table 30-2. Decoupling Requirements

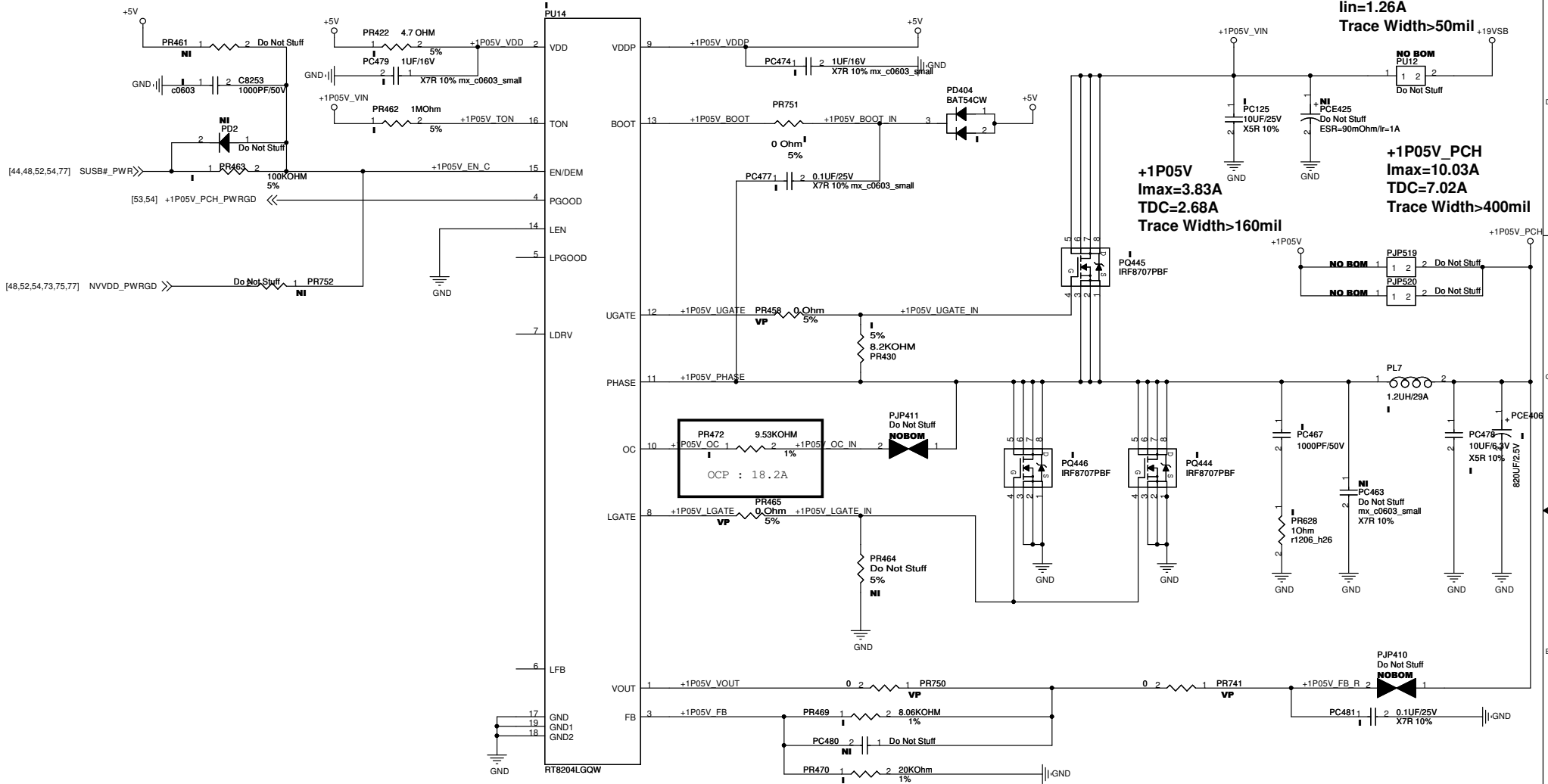
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2, 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

PL-CAP \*4 +2(NI)  
MLCC \*18 +3(NI)

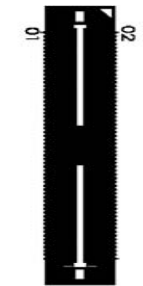




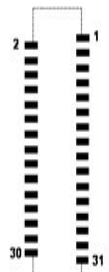




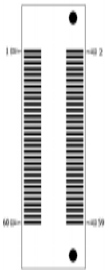
# INTEL PCH XDP DEBUG PORT



TOP SIDE VIEW

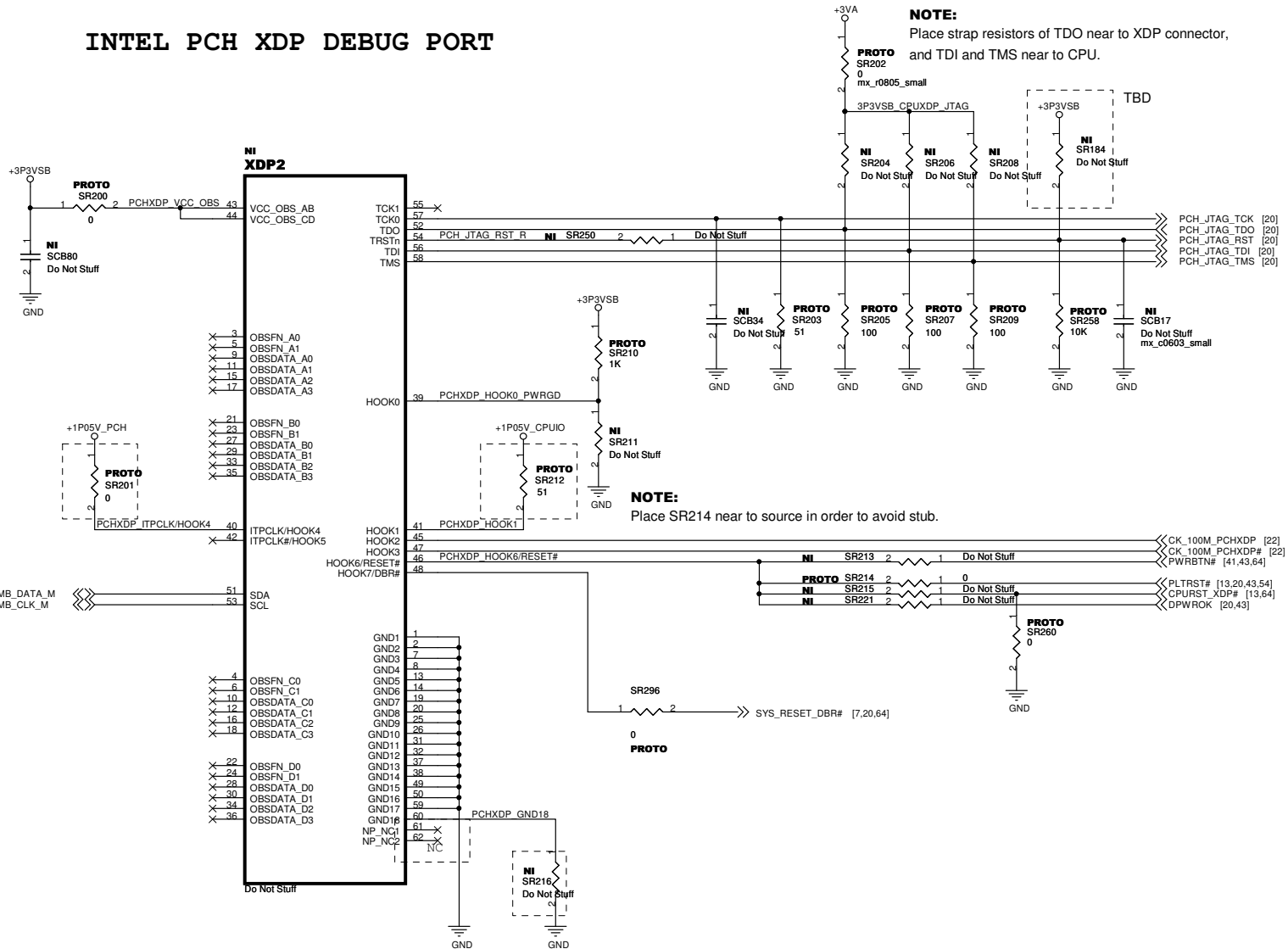


HR8/DF9C-318-1V(22)  
PCB FOOTPRINT



BOTTOM SIDE VIEW

[10,11,37,38,45,64,79] SMB\_DATA\_M  
[10,11,37,38,45,64,79] SMB\_CLK\_M





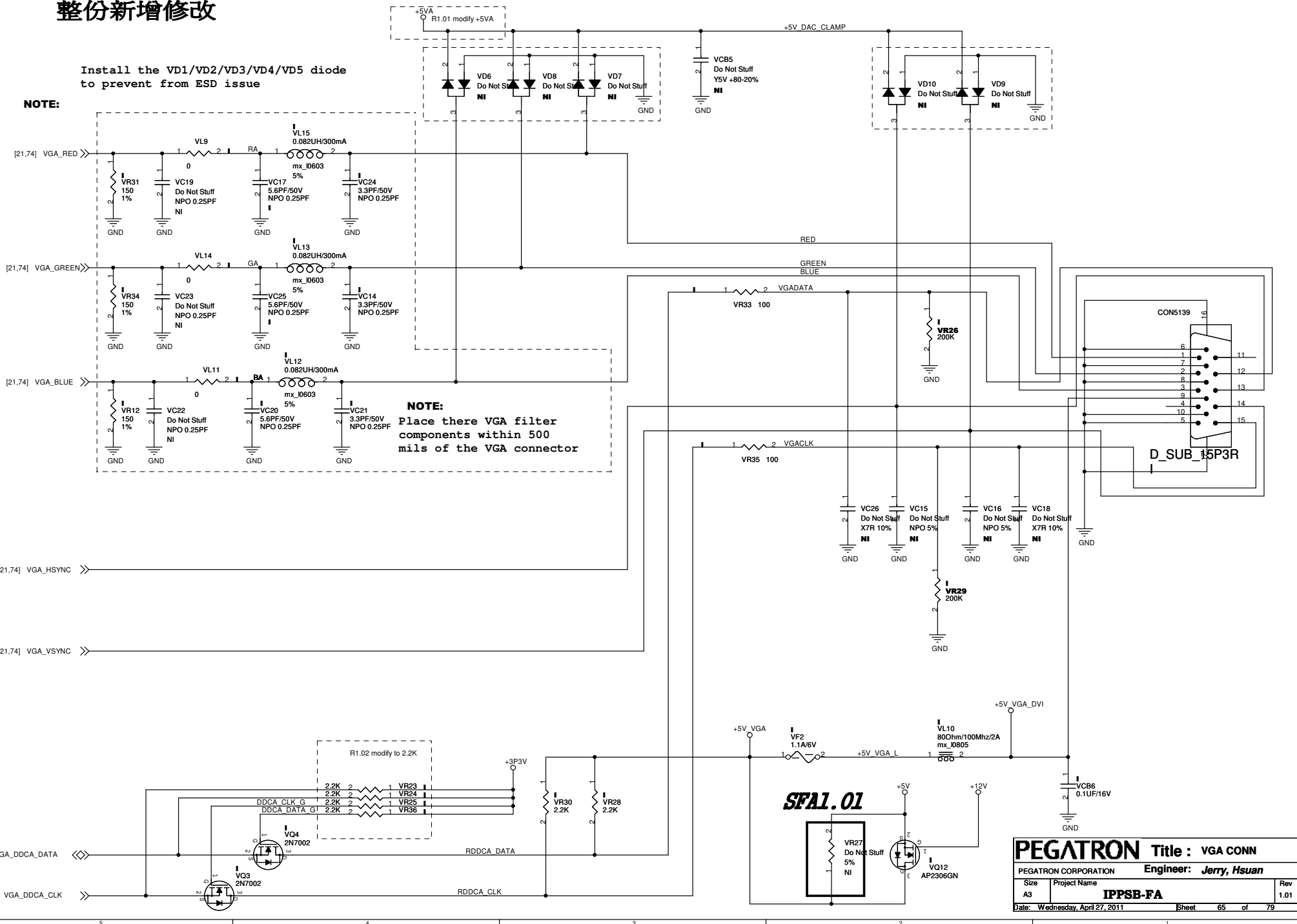
\_\_\_\_\_ 1



## 整份新增修改

Install the VD1/VD2/VD3/VD4/VD5 diode to prevent from ESD issue

**NOTE:**



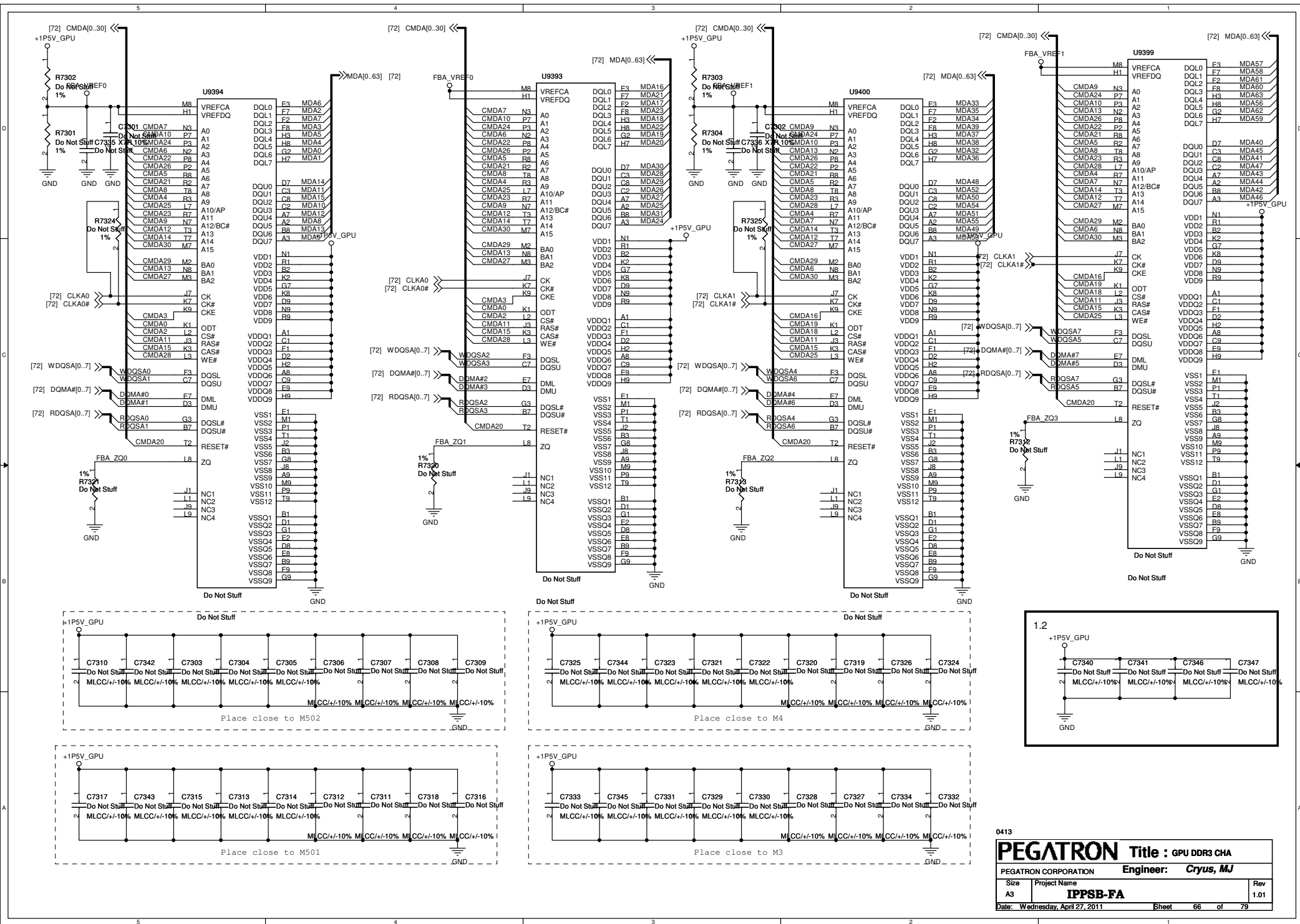
***SFA1.01***

**PEGATRON** Title : VGA CONN

PEGATRON CORPORATION      **Engineer:** *Jerry, Hsuan*

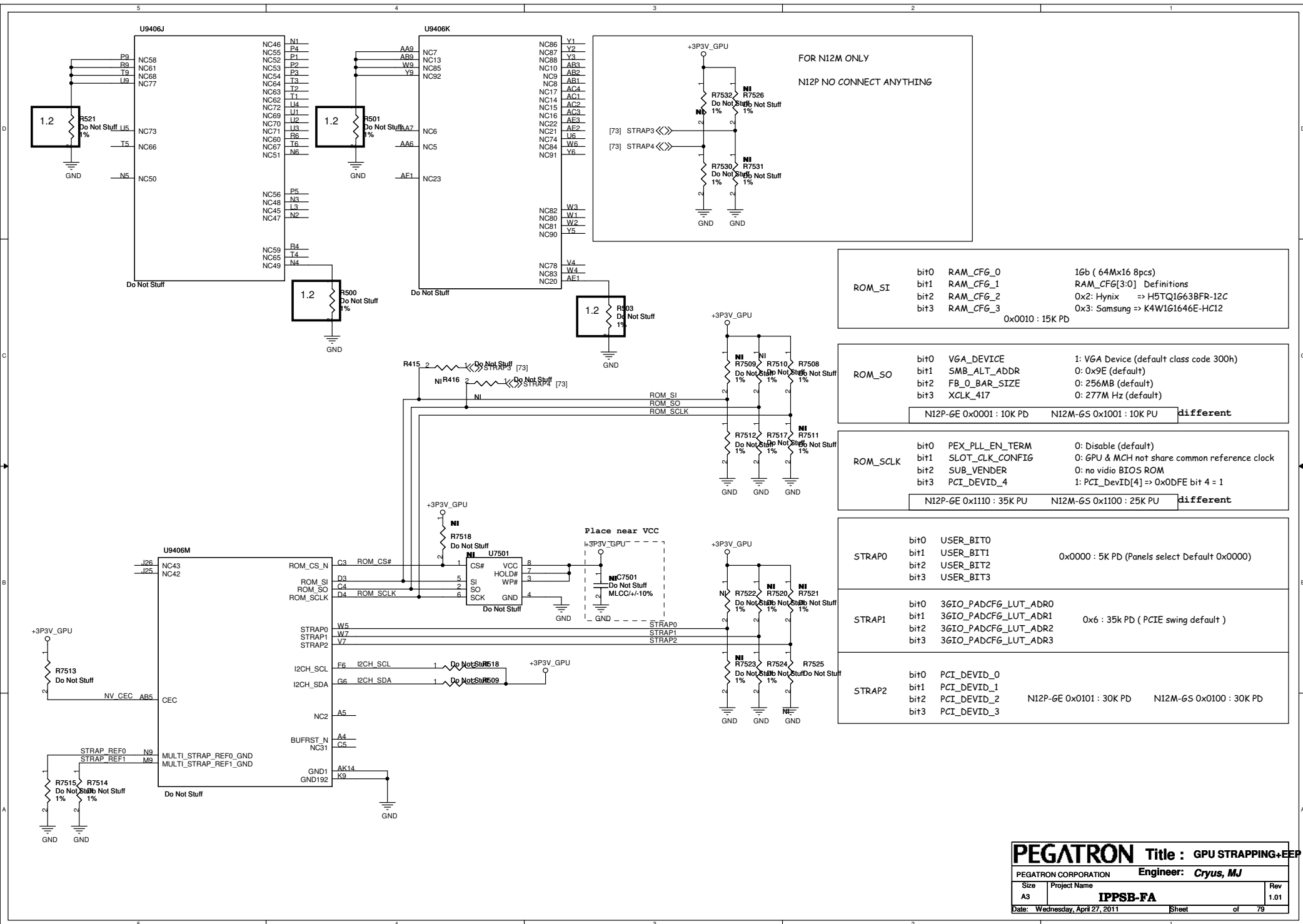
Size A3	Project Name <b>IPPSB-FA</b>	Rev 1.01
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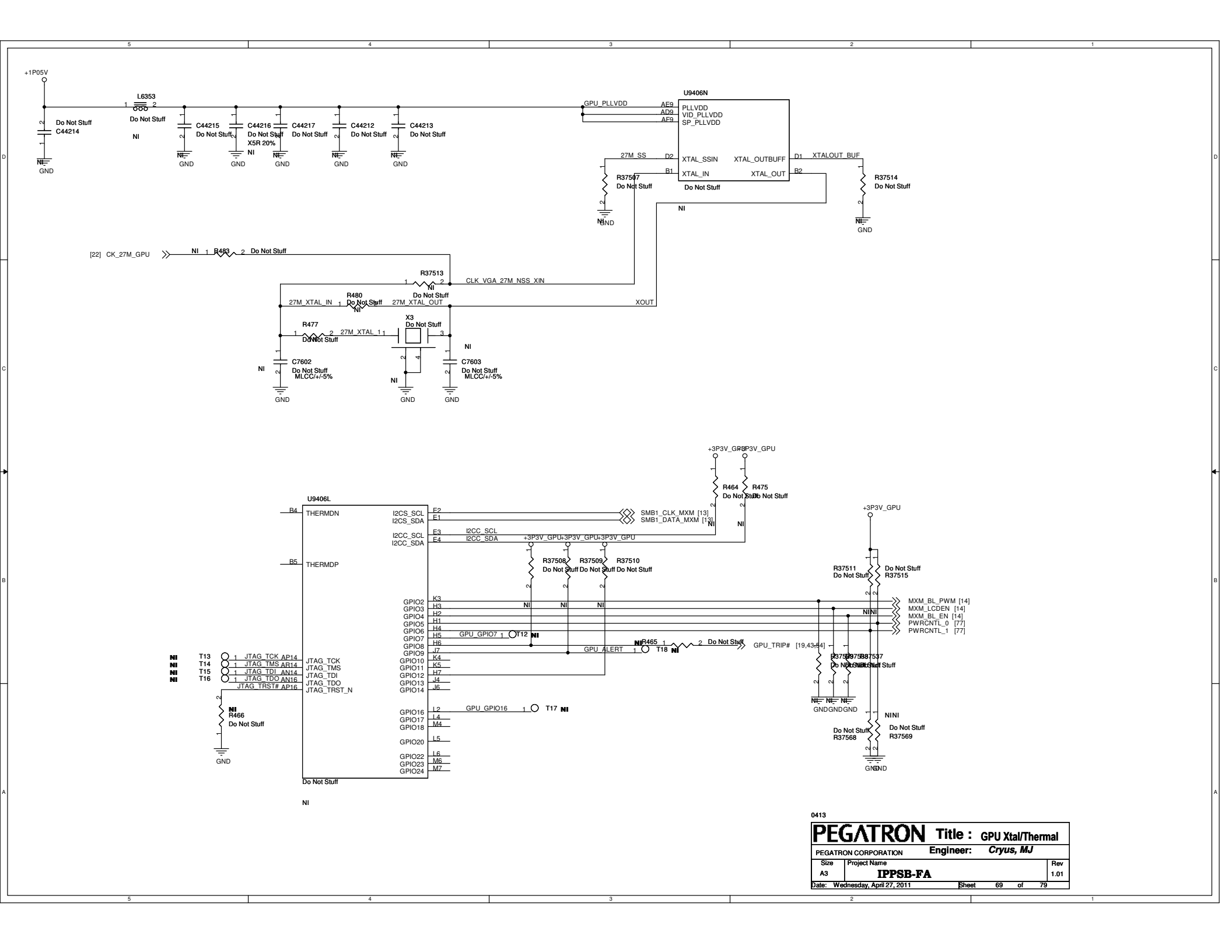
Date: Wednesday, April 27, 2011 Sheet 65 of 79

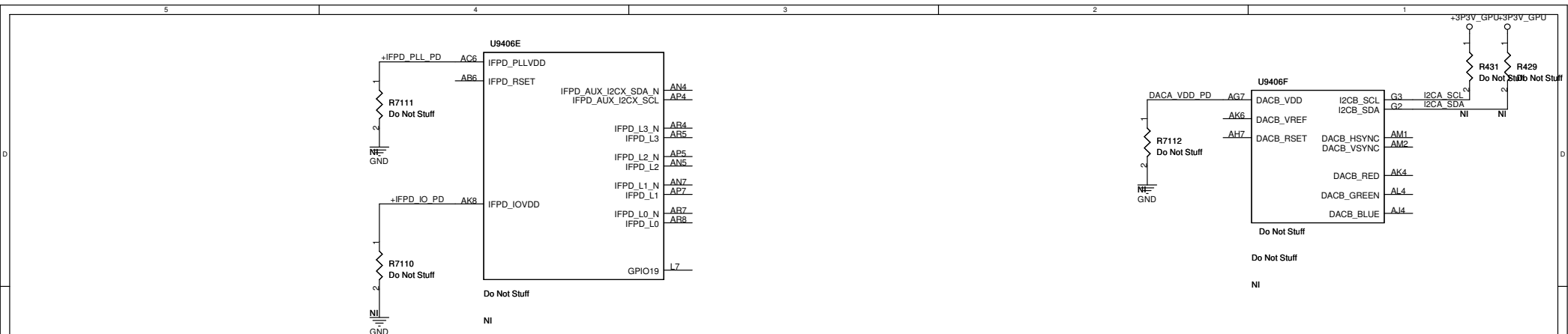


0413

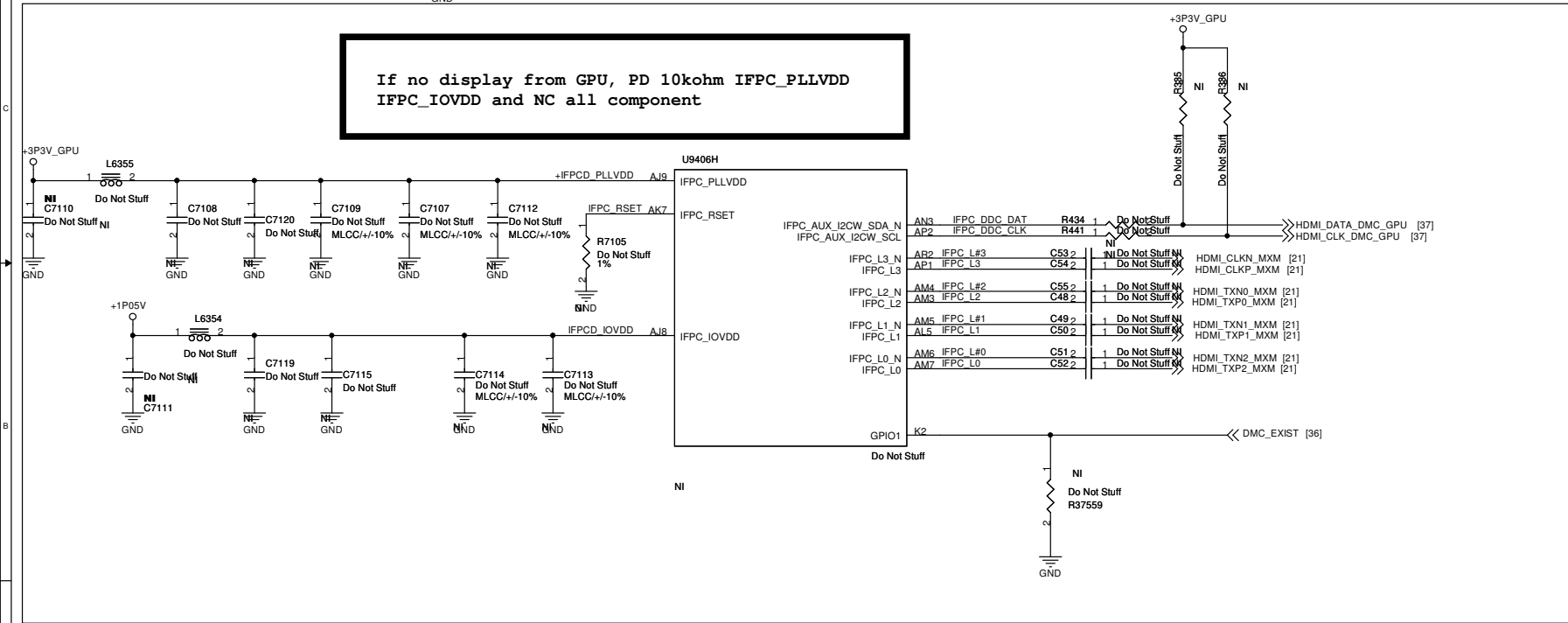






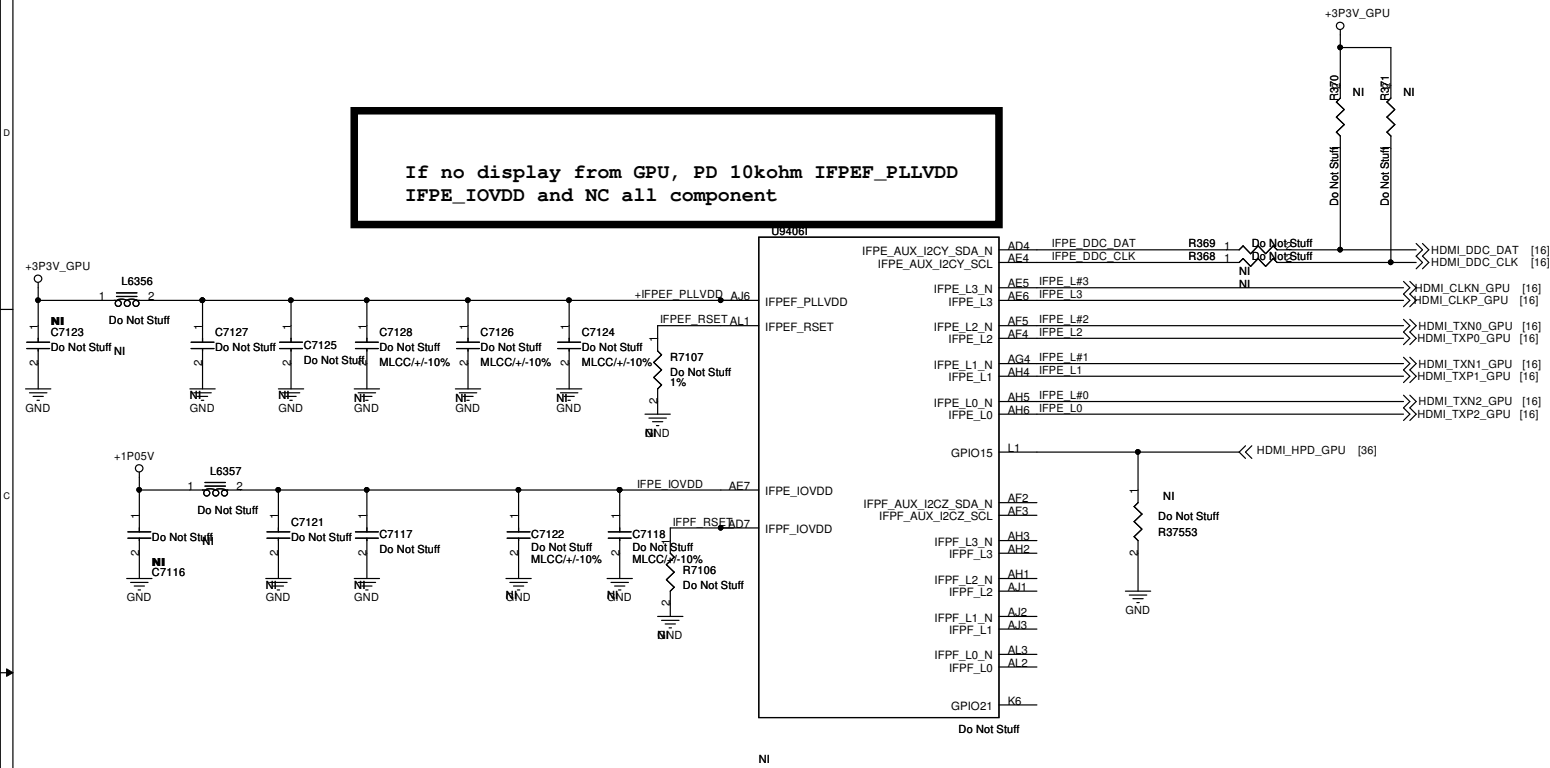


If no display from GPU, PD 10kohm IFPC\_PLLVDD  
IFPC\_IOVDD and NC all component



0413

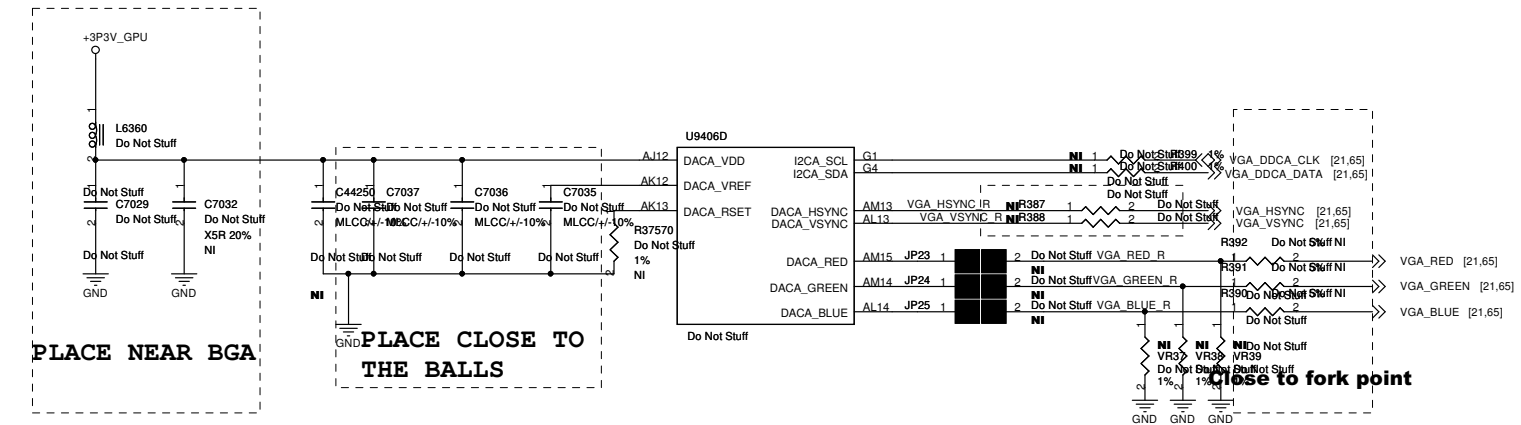
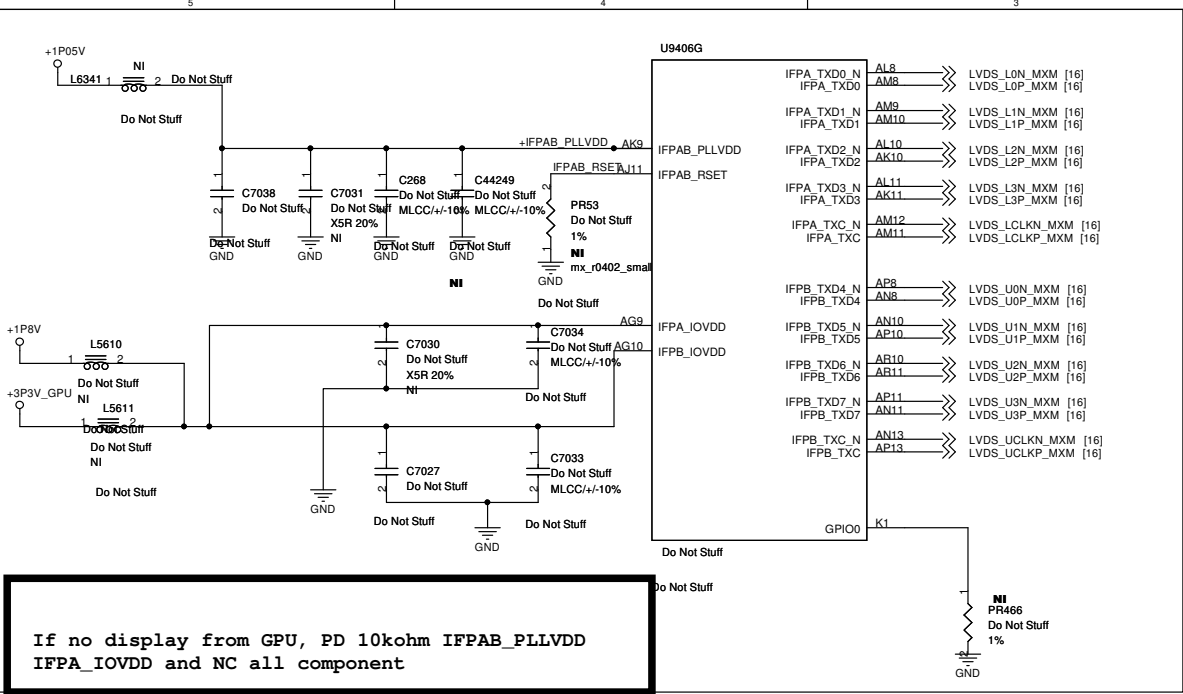
If no display from GPU, PD 10kohm IFPEF\_PLLVDD  
IFPE\_IOVDD and NC all component



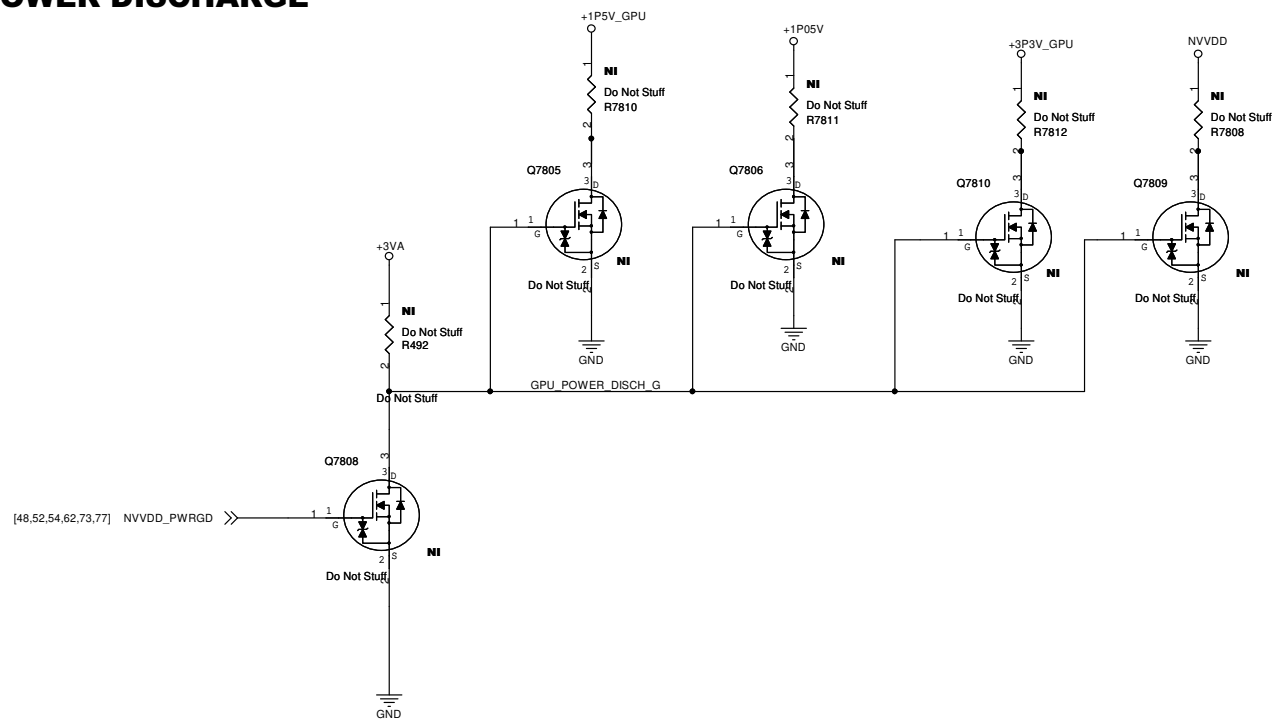








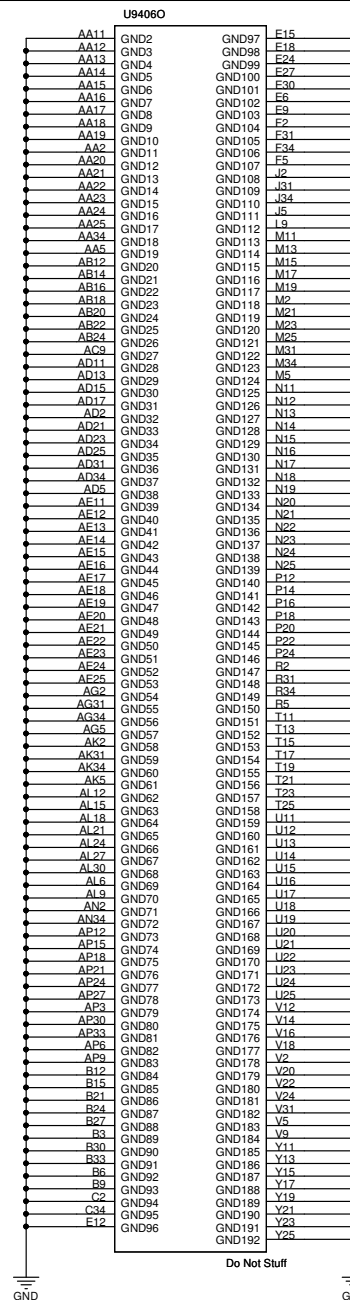
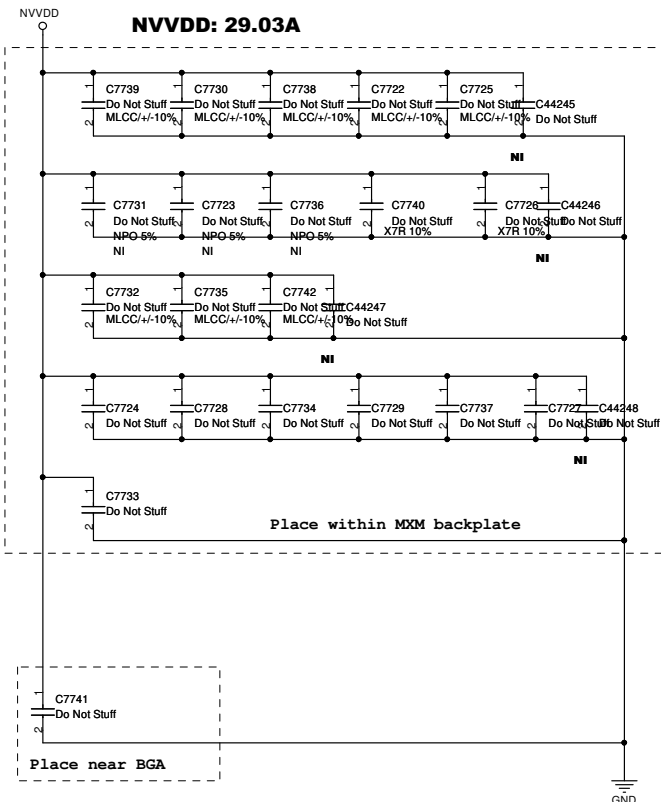
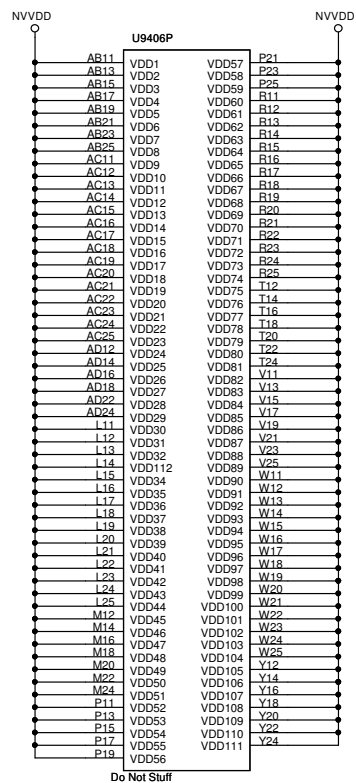
## GPU POWER DISCHARGE



0413

<b>PEGATRON</b>		<b>Title : GPU Discharge</b>	
PEGATRON CORPORATION		<b>Engineer: Cryus, MJ</b>	
Size A3	Project Name <b>IPPSB-FA</b>	Rev 1.01	
Date: Wednesday, April 27, 2011		Sheet	75 of 79

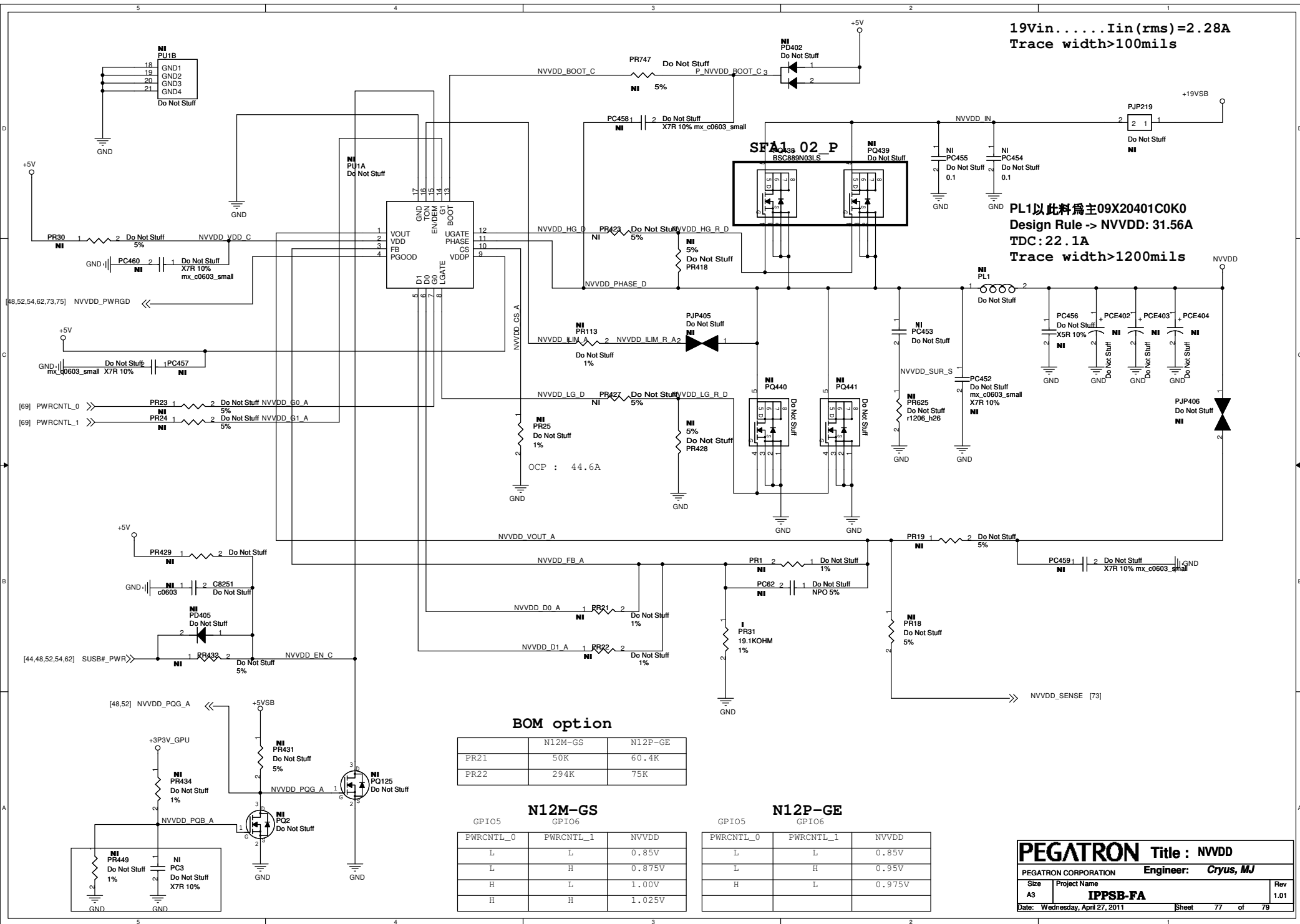
12/28 新增  
01/07 修改

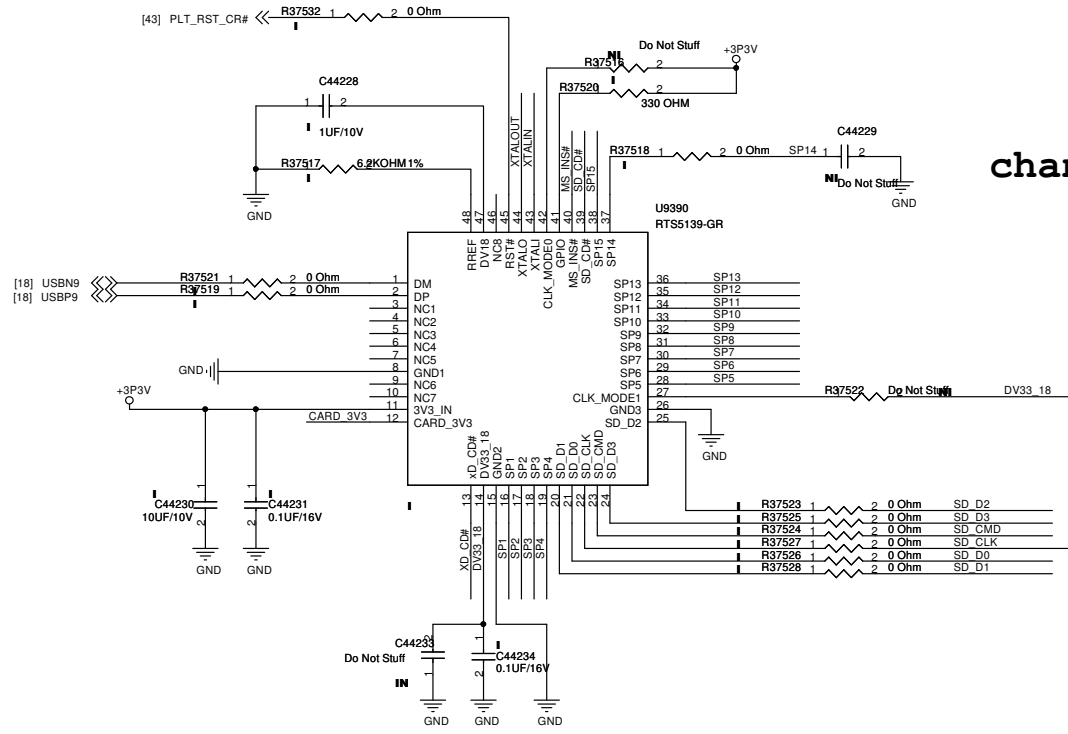


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : GPU POWER&GND

PEGATRON CORPORATION		Engineer: Cryus, MJ	
Size A3	Project Name  IPPSB-FA	Rev 1.01	
Date: Tuesday, April 26, 2011		Sheet 76 of 79	

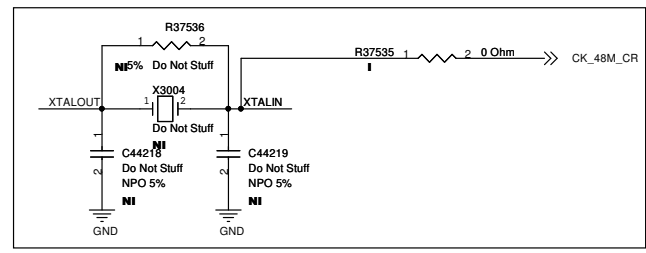




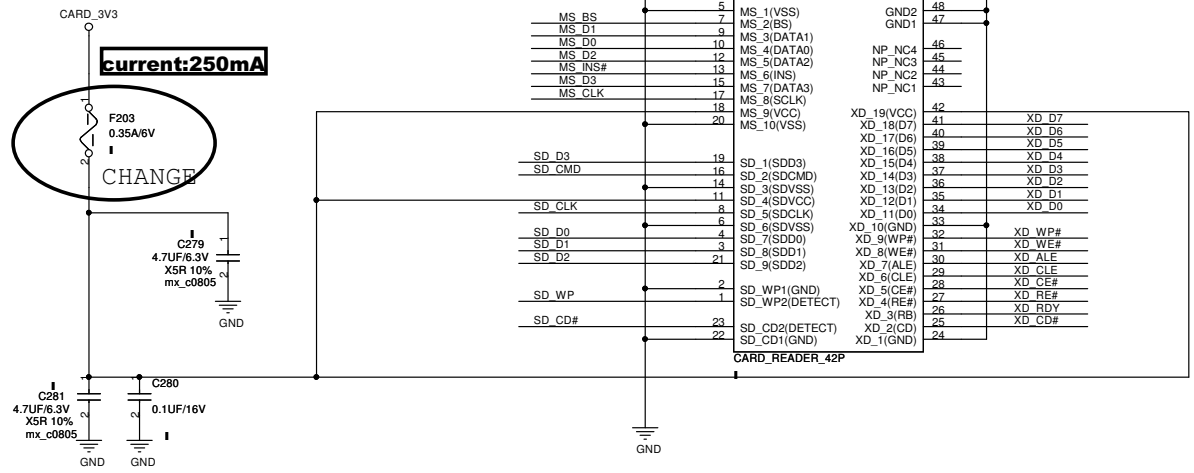
change 48M crystal

SHARE PINGS

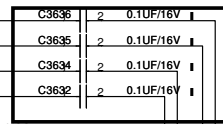
SP1	SD D7	XD RDY
SP2	SD D6	XD RE#
SP3	SD D5	XD CE#
SP4	SD D4	XD WE#
SP5		MS BS
SP6	MS D5	XD ALE
SP7	MS D1	XD WP#
SP8	MS D4	XD D0
SP9	MS D0	XD D1
SP10	MS D2	XD D2
SP11	MS D6	XD D3
SP12	MS D3	XD D4
SP13	MS D7	XD D5
SP14		MS CLK
SP15	SD WP	XD D7



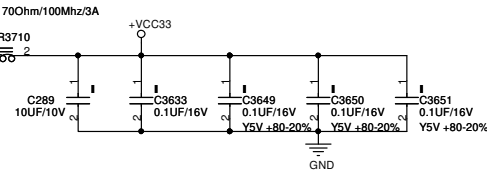
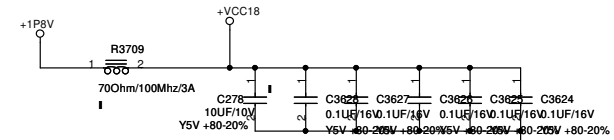
# Scott CardReader IO



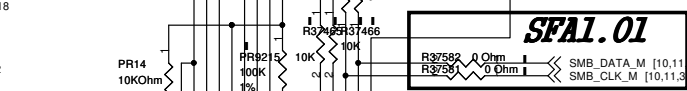
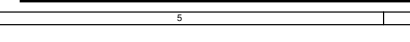
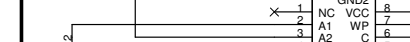
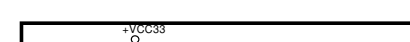
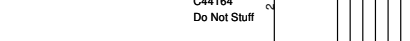
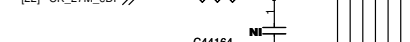
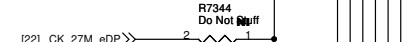
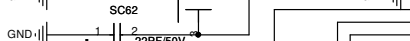
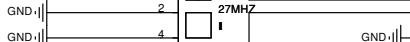
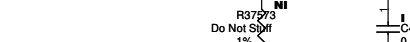
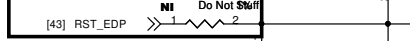
[21] EDP0\_PCH\_D >>  
[21] EDP0#\_PCH\_D >>  
[21] EDP1\_PCH\_D >>  
[21] EDP1#\_PCH\_D >>



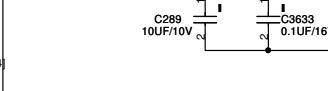
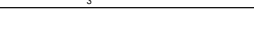
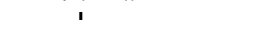
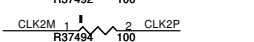
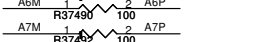
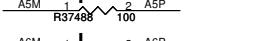
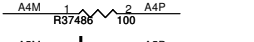
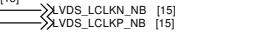
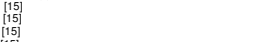
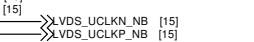
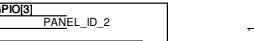
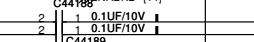
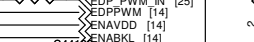
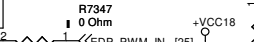
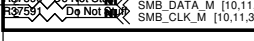
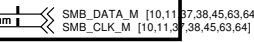
**SFAL.04**



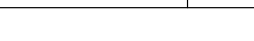
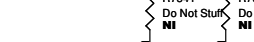
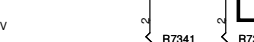
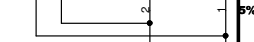
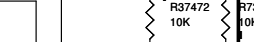
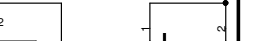
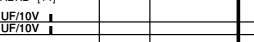
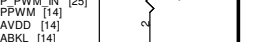
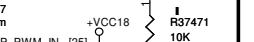
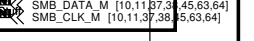
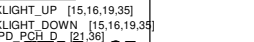
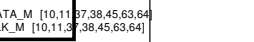
**SFAL.01**



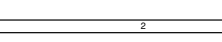
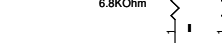
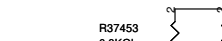
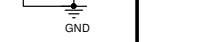
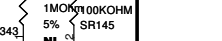
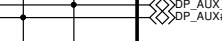
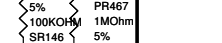
**SFAL.01**



**SFAL.01**



**SFAL.04**



**SFAL.01**

